3.0 General Considerations for IGBT and Intelligent Power Modules

Powerex IGBT and Intelligent Power Modules are based on advanced low loss IGBT and free-wheel diode technologies. The general guidelines for power circuit, snubber and thermal system design are essentially the same for both product families. This section will cover these general application issues. The sections that follow will give specific details for each product family.

3.1 Numbering System

(1) Devices:
CM = IGBTMOD™,
PM = INTELLIMOD™

(2) Current Rating I_C (Amperes)

(3) For INTELLIMOD™:
H = Single
D = Dual
C = Six in one
R = Seven in one

(4) IGBTMOD™:
H = Single
D = Dual
T = Six
E3 = Chopper
B = Four in one

(5) Outline or Minor Change
U = U-Package

(6) For IGBTMOD™:
Voltage, V_{CES} Volts (x50)

(7) For INTELLIMOD™:
Voltage V_{CES} Volts (x10)

(8) For IGBTMOD™:
F = Trench Gate
H = Total Performance H-Series IGBTMOD™ Module
K = Non-epitaxial Punch Through

For INTELLIMOD™
S = Third Generation
V = V-Series

Examples:

CM 100 D Y – 24 H
(1) (2) (4) (5) (6) (8)

CM100DY-24H is a 100 Ampere, 1200 Volt, Dual IGBTMOD™ Module

PM 600 H SA 120
(1) (2) (3) (8) (5) (7)

PM600HSA120 is a 600 Ampere, 1200 Volt, Single INTELLIMOD™ Module

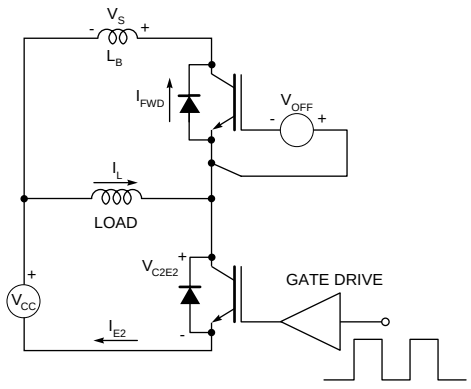
3.2 Power Circuit Design

In high power systems rapid turn-on and turn-off operations produce harsh dynamic conditions. The power circuit, snubbers, and gate drive must be designed to deal with extreme di/dt and dv/dt stresses. Excessive transient voltages can occur if leakage inductance in the power circuit and snubbers is not minimized. Ground loops and capacitive coupling can cause serious noise problems. An appropriate mechanical and electrical layout is essential for reliable and efficient operation of IGBT and Intelligent Power Modules.

3.2.1 Turn-off Surge Voltage

Turn-off surge voltage is the transient voltage that occurs when the current through the IGBT is interrupted at turn-off. To examine this, consider the inductive load half-bridge circuit shown in Figure 3.1. In this test circuit the top IGBT is biased off and the bottom device is switched on and off with a burst of pulses. Each time the lower device is turned on, the current in the inductive load (I_L) will increase. When the lower device is turned off, the current in the inductive load cannot change instantly. It must circulate through the free-wheel diode of the upper device. When the lower device turns back on, the load current will commutate back to the lower device and begin to ramp up again. If the circuit was ideal and had no parasitic inductance, the voltage across the lower device (V_{C2E2}) at turn-off would increase until it reached one diode drop above the bus voltage (V_{CC}). The upper device's free-wheel diode would then turn on stopping the voltage from increasing further. Unfortunately real power circuits have parasitic leakage inductance. In Figure 3.1 a lump inductance (L_B) has been added to the half-bridge circuit to simulate the effect of parasitic bus inductance. When the lower device turns off the inductance L_B resists the commutation of the load current to the free-wheel diode of the upper device. A voltage (V_S) equal to L_B x di/dt appears across L_B in opposition to increasing current in the bus. The polarity of this voltage is such that it adds to the DC bus voltage and appears across the lower IGBT as a surge voltage. In extreme cases, the surge voltage can exceed the IGBT's V_{CES} rating and cause it to fail. In a real application the parasitic inductance (L_S) is distributed throughout the power circuit but the effect is the same.

Figure 3.1 Half-bridge Circuit with Parasitic Bus Inductance



3.2.2 Free-wheel Diode Recovery Surge

A surge voltage similar to the turn-off surge can occur when the free-wheel diode recovers. Assume that the lower IGBT in Figure 3.1 is off and that the load current (I_L) is circulating through the free-wheel diode of the upper IGBT. When the lower device turns on, the current in the free-wheel diode of the upper device (I_{FWD}) decreases as the load current begins to commutate to the lower device and becomes negative during reverse recovery of the free-wheel diode. When the free-wheel diode recovers, the current in the bus is quickly decreased to zero. The situation is similar to the turn-off operation described in Section 3.2.1. The parasitic bus inductance (L_B) develops a surge voltage equal to L_B x di/dt in opposition to the decreasing current. In this case, the di/dt is related to the recovery characteristic of the free-wheel diode. Some fast recovery diodes can develop extremely high recovery di/dt when they are hard recovered by the rapid turn on of the lower IGBT. This condition, commonly referred to as "snappy" recovery, can cause very high transient voltages. Powerex IGBT

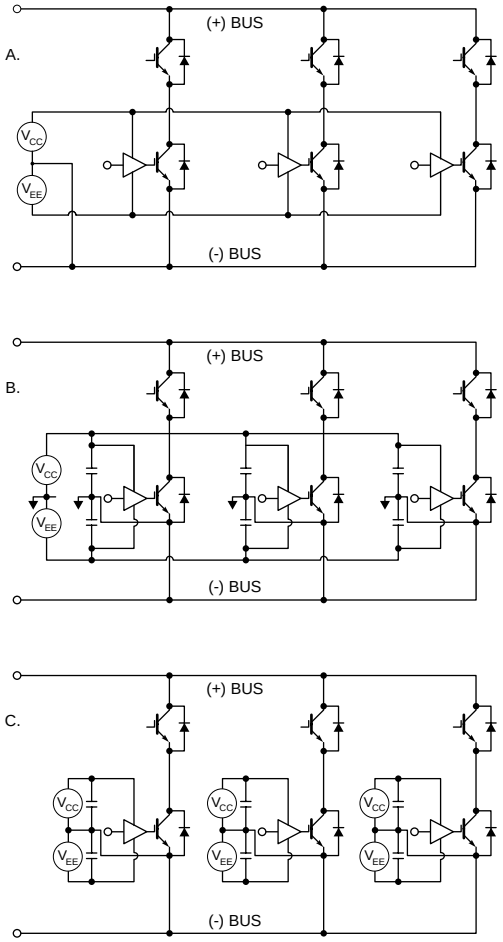
modules have a specially optimized, ultra fast, soft recovery free-wheel diode that virtually eliminates problems with snappy recovery.

3.2.3 Ground Loops

Ground loops are caused when gate drive or control signals share a return current path with the main current. During switching, voltage is induced in power circuit leakage inductance by the high di/dt of the main current. When this happens, points in the circuit that should be at “ground” potential may in fact be several volts above ground. This voltage can appear on the gates of devices that are supposed to be biased off causing them to turn on. In order to avoid this problem, careful referencing of gate drive and control circuits is required. In applications using large IGBT modules high di/dts make it increasingly difficult to avoid ground loop problems.
Figure 3.2A shows a circuit with potential ground loop problems. In this circuit the ground return for the gate drive passes through the main power bus. This circuit is suitable for use with low current six-pack devices because they have minimal inductance in the negative bus and a relatively low power circuit di/dt. However, even in this case a strong off-bias of -5 to -15V is recommended. *[Note 1]* At higher operating currents, voltages induced in the bus during switching are likely to cause
ground loop noise problems in the circuit of Figure 3.2A. Figure 3.2B shows the recommended connection of low side drivers using a single gate drive power supply. In this circuit, ground loop noise is minimized through the use of auxiliary emitters and local power supply decoupling capacitors. This circuit is suitable for use with modules rated up to about 200A. Figure 3.2C shows the recommended circuit for IGBT modules rated 300 amps or more. In this circuit separate isolated power supplies are used for each low side gate driver in order to eliminate ground loop problems.

Note 1. *In the case of the IPM a negative bias is not necessary.*

Figure 3.2 Avoiding Ground Loop Noise

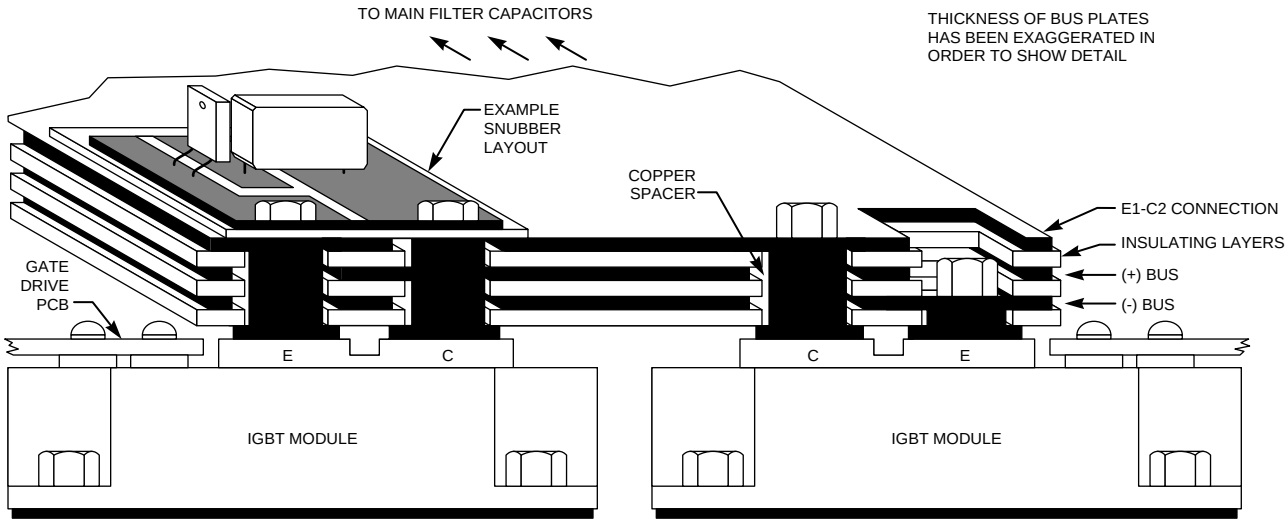


3.2.4 Reducing Power Circuit Inductance

The energy that causes transient voltages in IGBT power circuits is proportional to $1/2L_Si^2$. Here, L_S is the parasitic bus inductance and i is the operating current.

An important fact to remember is that this energy is proportional to the square of the operating current. Therefore, high current devices will require much lower power circuit inductance.

Figure 3.3 Cross-section of a Laminated Bus Structure



This presents a challenge to the IGBT circuit designer because the physical size and thermal requirements of these devices make longer power circuit connections necessary. With conventional buswork, these longer connections will cause more parasitic inductance making snubber design very difficult.

In order to obtain the low bus inductance recommended for high current applications, special bus structures are required. Laminated busses consisting of alternate copper plates and insulating layers can be designed with very low inductance. In a laminated bus, wide plates separated by insulating layers are used for the positive and negative bus connections. The wide plates act to cancel parasitic inductance in the power circuit. For absolute minimum bus inductance wide positive and negative bus plates are used to connect the IGBTs to the main capacitor bank.

Figure 3.3 shows the cross section of an inverter pole constructed using a laminated bus. In this structure the inductance in the E1 to C2 connection is minimized using another wide plate in the stack. Figure 3.4 shows an example layout for a large three phase inverter. This drawing also shows a large plate being used to make the series connection of the main bus capacitors for 460VAC applications.

3.3 Snubber Design

Snubber circuits are usually used to control turn-off and free-wheel diode recovery surge voltages. In some applications snubber circuits are used to reduce switching losses in the power device. General recommendations for snubbers are not possible to make because the type of snubber needed and component values required are highly dependent on the power circuit layout. In addition factors such as cost and operating frequency must be considered when selecting the best snubber for a given application.

The function of IGBT snubbers is different from classical bipolar transistor snubbers in two ways. First, Powerex IGBTs have strong switching SOAs. The snubber is not required to protect against RBSOA violations to the extent that it was with Darlington transistors. It is only necessary for the snubber to control transient voltages. Second, IGBTs are often operated at considerably higher frequencies than Darlingtons. Snubbers that are discharged through the device on every switching cycle dissipate too much power for these applications.

3.3.1 Snubber Types

Figure 3.5 shows four common IGBT snubber circuits. Snubber circuit “A” consists of a single low inductance film capacitor connected from C1 to E2 on a dual

Figure 3.4 Example Layout for a High Current 3-Phase Inverter

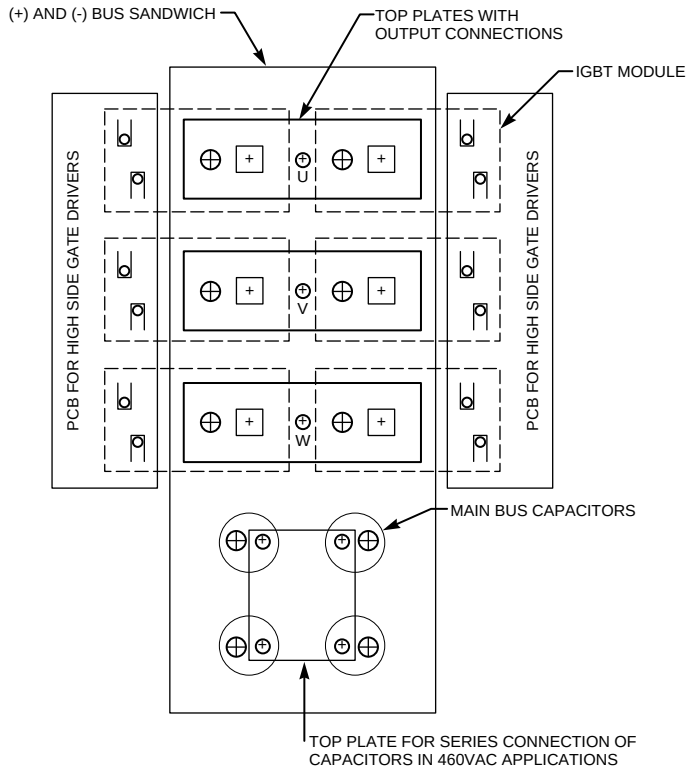
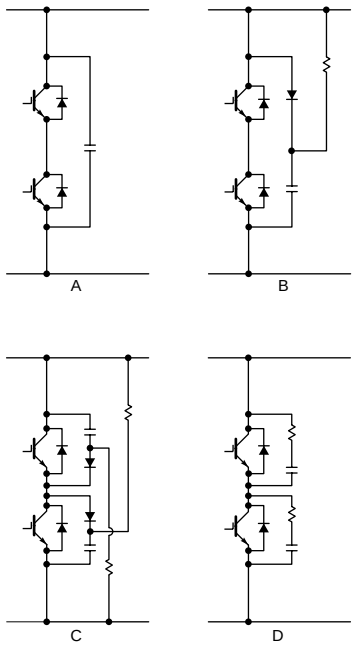


Figure 3.5 Common IGBT Snubber Circuits



IGBT module or from P to N on a six pack module. In low power designs this snubber will often provide effective, low cost control of transient voltages. As power levels increase, snubber "A" may begin to ring with parasitic bus inductance, Snubber "B" solves this problem by using a fast recovery diode to catch the transient voltage and block oscillations. The RC time constant of snubber "B" should be approximately one third of the switching period (τ = T/3 = 1/3f). With large IGBTs operating at high power levels, the parasitic loop inductance of snubber "B" may become too high for it to effectively control transient voltages. In these high current applications snubber "C" is usually used. This snubber functions similarly to "B" but it has lower loop inductance because it is connected directly to the collector and emitter of each IGBT. Snubber "D" is useful for controlling transient voltages, parasitic oscillations, and dv/dt noise. Unfortunately its losses are quite high and it is generally not suitable for high frequency applications. In very high power IGBT circuits, it is often helpful to use a small snubber "D" in conjunction with a main snubber "C" in order to help control parasitic oscillations in the main snubber loop. In very high power applications it may be helpful to combine types "A" and "C" in order to reduce the stresses on the snubber diode.

3.3.2 Effect of Snubber Inductance

Figure 3.6 shows a typical turn-off voltage waveform using snubber "C" of Figure 3.5. The initial voltage spike (ΔV_1) is caused by a combination of the parasitic inductance in the snubber circuit and the forward recovery of the snubber diode. If a fast IGBT snubber diode is used the majority of this spike will be due to the inductance of the snubber. In this case, we can compute the magnitude of ΔV_1 using Equation 3.1.

Equation 3.1

$$\Delta V_1 = L_S \times di/dt$$

Where:

L_S = Parasitic Snubber Inductance
di/dt = Turn-off or diode recovery di/dt

In a typical IGBT power circuit the di/dt will approach 0.01A/ns x I_C. If a limit value for ΔV_1 is established then this di/dt can be used to estimate the maximum allowable snubber inductance. For example, assume that we have an IGBT power circuit that will operate at a peak current of 400A and that ΔV_1 must be limited to 100V. The worst case di/dt is approximately:

$$di/dt = 0.01A/ns \times 400A = 4A/ns$$

Solving Equation 3.1 for L_S we get:

$$L_S = \Delta V_1 \div di/dt = 100V \div 4A/ns = 25nH$$

From the computations above, it is clear that high power IGBT circuits will require very low inductance snubbers. Snubbers must be connected as close as possible to the IGBT module. Parasitic inductance inside snubber diode packages and in the leads of snubber capacitors must be considered when designing snubbers. Often smaller paralleled capacitors and diodes will yield lower inductance than single larger ones. Designing an IGBT power circuit with minimum bus inductance will also help because smaller lower inductance snubber components can be used.

3.3.3 Effect of Bus Inductance

After the initial surge in Figure 3.6 the transient voltage begins to rise again as the snubber capacitor charges. The peak of this second rise (ΔV_2) is a function of the snubber capacitor value and the parasitic bus inductance. In order to estimate the magnitude of ΔV_2 we can apply the Law of Conservation of Energy to obtain Equation 3.2.

Equation 3.2

$$1/2\ L_B i^2 = 1/2\ C\Delta V_2^2$$

Where:

L_B = Parasitic Bus Inductance
i = Operating Current
C = Value of Snubber Capacitor
ΔV_2 = Peak Snubber Voltage

If we establish a limit for ΔV_2, then we can calculate the value of snubber capacitor that will be needed for a given power circuit by solving Equation 3.2 for C.

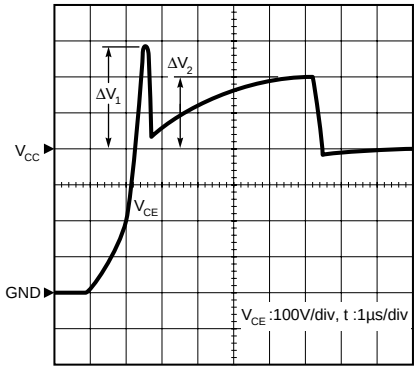
Equation 3.3

$$C = L_B i^2 \div \Delta V_2^2$$

Analysis of Equation 3.3 reveals that the value of the required capacitor is directly proportional to the value of the parasitic bus inductance. The methods to reduce bus inductance described in Section 3.2.4 therefore permit a reduction in the required snubber capacitor.

A second consideration is that the value of the capacitor is directly proportional to the square of the current being turned off. This is significant as this current can be very high during short circuit unless the limitation techniques described in Section 4.7.2 are employed. The suggested snubber design values given in Table 3.1 assume that these techniques have been used and that only normal current requirements up to maximum overload have to be handled.

Figure 3.6 Typical Turn-off Voltage Waveform Using a Snubber



A final consideration is that the value of snubber capacitance is inversely proportional to the square of the magnitude of the allowed spike voltage over the bus voltage. Therefore, allowing a reduced margin between the peak of the voltage spike and the V_{CES} rating may permit a significant reduction in the required value of snubber capacitor. The suggested snubber design values given in Table 3.1 are based on 100 Volt overshoot.

3.3.4 Power Circuit and Snubber Recommendations

Table 3.1 lists suggested targets for the main DC bus inductance. These values are chosen in order to allow design of manageable snubbers while maintaining good control over transient voltages.

Assuming that the target bus inductance has been met, it is

possible to suggest snubber types and assign values to the snubber capacitors. In applications using six-in-one or seven-in-one (6-pack or 7-pack) type modules, it is usually possible to use a single low inductance capacitor connected across the P and N terminals as the snubber shown in Figure 3.5A. Similarly, on dual type modules a low inductance capacitor connected between the C1 and E2 terminals is usually sufficient for control of transient voltages. These configurations are shown in Figure 3.7. The capacitance needed in a given application is difficult to estimate. The capacitor must be made large enough to avoid sympathetic oscillations in the LC circuit formed by the capacitor and the parasitic DC bus inductance. Usually a capacitance of about 1μF per 100A of collector current is sufficient. The capacitor should be polypropylene film or a similar low loss dielectric and be mounted as close to the module's terminals as possible. Total snubber loop inductance including the capacitor's internal inductance should be minimized. If parasitic oscillations are a problem in the application, it may be necessary to use the snubber shown in Figure 3.5B.

With high current single IGBT modules a single bus decoupling capacitor alone is usually insufficient for control of transient voltages. In these applications a clamp type RCD circuit like the one shown in Figure 3.5C is usually used. In this circuit the snubber capacitors are charged to the DC bus voltage through the resistors. When the IGBT turns off, parasitic inductance in the DC bus causes a transient voltage across the IGBT. As soon as the voltage exceeds the DC bus voltage the snubber diode turns on and diverts the energy stored in the parasitic bus inductance into the snubber capacitor. This snubber controls transient voltages better than the snubbers shown in Figure 3.7 since it eliminates the inductance of the opposite IGBT package and the E1 to C2 connection from the snubber loop. This clamp type snubber circuit is typically constructed on a small printed circuit board using axial or radial leaded capacitors along with the fast recovery snubber diodes and power resistors. The circuit board is then mounted to the bus bars directly above the IGBT module. (See Figure 3.3) Capacitor and

Figure 3.7 Snubber Circuits for 6-Pack, 7-Pack, and Dual Type Modules

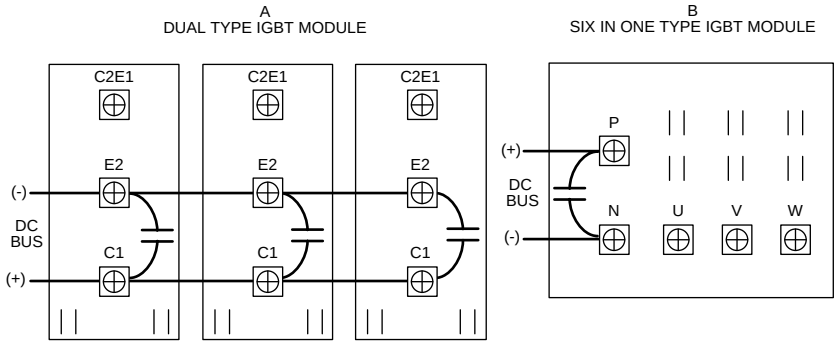


Table 3.1 Snubber and Power Circuit Design Recommendations

Module Type	Suggested Design Values				
	Main Bus	Snubber Type (Figure)	Snubber Loop Inductance	Snubber Capacitor Value	Snubber Diode
10A-50A 6-Pack and 7-Pack Types	200nH	3.7B	20nH	0.1-0.47μF	n/a
75A-200A 6-Pack and 7-Pack Types	100nH	3.7B	20nH	0.6-2.0μF	n/a
50A-200A Dual Types	100nH	3.7A	20nH	0.47-2.0μF	n/a
300A-600A Dual Types*	50nH	3.7A	20nH	3.0-6.0μF	n/a
200-300A Single Types	50nH	3.5C	30nH-15nH	0.47μF	600V: RM50HG-12S 1200V: RM25HG-24S
400A Single Type	50nH	3.5C	12nH	1.0μF	600V: RM50HG-12S 1200V: RM25HG-24S (2 Parallel) 1400V, 1700V: RM35HG-34S (2 Parallel)
600A-1000A Single Type	50nH	3.5C	8nH	2.0μF	600V: RM50HG-12S (2 Parallel) 1200V: RM25HG-24S (3 Parallel) 1400V: RM35HG-34S (3 Parallel)

*At high DC bus voltages it may be necessary to use the snubber shown in Figure 3.5C for these high current dual types. In this case use the recommendations given for single types.

diode recommendations for this type of snubber are shown in Table 3.1. In this case the capacitor values are derived using Equation 3.3 and assuming a transient voltage of 100V with the IGBT switching at rated current. In order to be effective the snubber must have low inductance. The effect of snubber inductance is covered in Section 3.3.2. Target values for snubber loop inductance based on a surge voltage of 100V are also given in Table 3.1.

3.4 Thermal Considerations

When operating the power devices contained in IGBT and Intelligent Power Modules will have conduction and switching power losses. The heat generated as a result of these losses must be conducted away from the power chips and into the environment using a heatsink. If an appropriate thermal system is not used the power devices will overheat which could result in failure. In many applications the maximum usable power output of the module will be limited by the systems thermal design.

3.4.1 Estimating Power Losses

The first step in thermal design is the estimation of total power loss. In power electronic circuits using IGBTs the two most important sources of power dissipation that must be considered are conduction losses and switching losses.

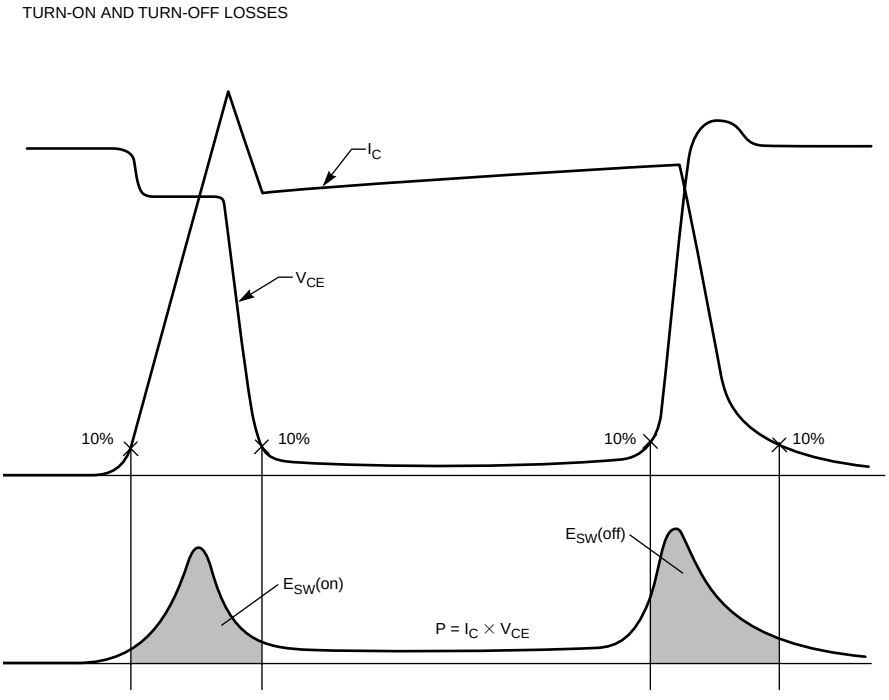
CONDUCTION LOSSES

Conduction losses are the losses that occur while the IGBT is on and conducting current. The total power dissipation during conduction is computed by multiplying the on-state saturation voltage by the on-state current. In PWM applications the conduction loss should be multiplied by the duty factor to obtain the average power dissipated. A first approximation of conduction losses can be obtained by multiplying the IGBT's rated $V_{CE}(SAT)$ by the expected average device current. In most applications the actual losses will be less because $V_{CE}(SAT)$ is lower than the data sheet value at currents less than rated I_C. When switching inductive loads the conduction losses for the free-wheel diode must be considered. Free-wheel diode losses can be approximated by multiplying the data sheet V_{FM} by the expected average diode current.

SWITCHING LOSSES

Switching loss is the power dissipated during the turn-on and turn-off switching transitions. In high frequency PWM switching losses can be substantial and must be considered in thermal design. The most accurate method of determining switching losses is to plot the I_C and V_{CE} waveforms during the switching transition. Multiply the waveforms point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy expressed in watt-seconds/pulse or J/pulse. The standard definitions of turn-on ($E_{SW(on)}$) and turn-off ($E_{SW(off)}$) switching energy is given in Figure 3.8. The waveform shown is typical of the hard switched

Figure 3.8 Switching Losses



clamped inductive load test that is used to generate all published switching energy data. The area is usually computed by graphic integration. Digital oscilloscopes with waveform processing capability will greatly simplify switching loss calculations. From Figure 3.8 it can be observed that there are pulses of power loss at turn-on and turn-off of the IGBT. The instantaneous junction temperature rise due to these pulses is not normally a concern because of their extremely short duration. However, the sum of these power losses in an application where the device is repetitively switching on and off can be significant. In cases where the operating current and applied DC bus voltage are constant and therefore $E_{SW(on)}$ and $E_{SW(off)}$ are the same for every turn-on and turn-off event the average switching power loss can be computed by taking the sum of $E_{SW(on)}$ and $E_{SW(off)}$ and dividing by the switching period T. Noting that dividing by the switching period is the same as multiplying by the frequency results in the most basic equation for average switching power loss:

$$P_{SW} = f_{SW} \times (E_{SW(on)} + E_{SW(off)})$$

Where:
f_{SW} is Switching Frequency
$E_{SW(on)}$ is turn-on switching energy
$E_{SW(off)}$ is turn-off switching energy

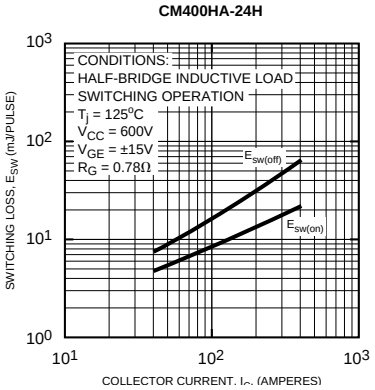
Figure 3.9 shows switching energy versus collector current for a 400A 1200V H-Series IGBT Module (CM400HA-24H). This curve is made using a half bridge test circuit with an inductive load. The turn-on loss includes the losses caused by the hard recovery of the opposite free-wheel diode. The critical conditions including junction temperature (T_j), DC bus voltage (V_{CC}), gate drive voltage V_{GE}, and series gate resistance (R_G) are given on the curve. Switching energy curves like this one are available for all Powerex IGBT and Intelligent Power Modules and most can be found in Sections 4.4.8 and 6.5.2 of this application note. Switching energy curves are very useful for initial loss estimation. In applications where the operating current and applied DC bus voltage are constant the average switching power loss can be computed by reading $E_{SW(on)}$ and $E_{SW(off)}$ from the curve at the operating current and using the equation given above. In applications where the current is changing such as in a sinusoidal output inverter the loss computation becomes more complex. In these cases it is necessary to consider the change in switching energy at each switching event over a fundamental cycle. A method for loss estimation in a sinusoidal output PWM inverter is given in Section 3.4.2. Final switching loss analysis should always be done with actual waveforms taken under worst case operating conditions.

The main use of the estimated power loss calculation is to provide a starting point for preliminary device selection. The final selection must be based on rigorous power and temperature rise calculations.

3.4.2 VVVF Inverter Loss Calculation

One common application of Power Modules is the variable voltage variable frequency (VVVF) inverter. In VVVF inverters, PWM modulation is used to synthesize sinusoidal output currents. In this application the IGBT current and duty cycle are constantly changing making loss estimation very difficult. The following equations can be used for initial loss estimation in VVVF applications. Actual losses will depend on temperature, sinusoidal output frequency, output current ripple and other factors. Figure 3.10 is a typical VVVF inverter circuit and output waveform.

Figure 3.9 Switching Energy vs. Collector Current



Equations for Power Loss Calculation for Sinusoidal Inverters

IGBT Loss

(1) Steady-state loss per switching IGBT

$$P_{SS} = I_{CP} \bullet V_{CE}(SAT) \bullet \frac{1}{2\pi}\int_0^{\pi} \sin^2 X \bullet \frac{1 + \sin(x+\theta)\bullet D}{2}\, dx = I_{CP} \bullet V_{CE(SAT)} \bullet \left(\frac{1}{8} + \frac{D}{3\pi}\cos\theta\right)$$

(P.F. = $\cos\theta$)

(2) Switching Loss per switching IGBT

$$P_{SW} = (E_{SW(on)} + E_{SW(off)}) \bullet f_{SW} \frac{1}{2\pi}\int_0^{\pi} \sin x\, dx = (E_{SW(on)} + E_{SW(off)}) \bullet f_{SW} \frac{1}{\pi}$$

(3) Total loss per IGBT

$$P_Q = P_{SS} + P_{SW}$$

Diode Loss

(1) Steady-state loss per diode

$$P_{DC} = I_{EP} \bullet V_{EC} \bullet \left(\frac{1}{8} - \frac{D}{3\pi}\cos\theta\right)$$

(2) Recovery Loss per Diode

$$P_{RR} = 0.125 \bullet I_{RR} \bullet t_{RR} \bullet V_{CE}(pk) \bullet f_{SW}$$

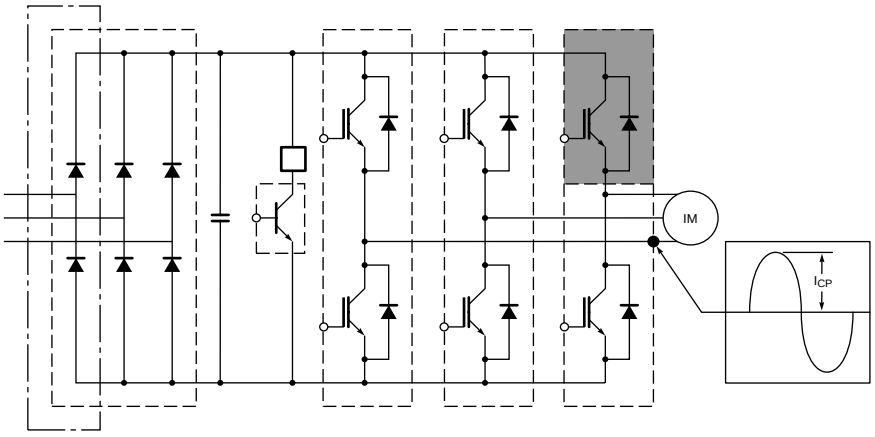
Loss per Arm (shaded part)

$$P_A = P_Q + P_D = P_{SS} + P_{SW} + P_{DC} + P_{RR}$$

Symbology:

$E_{SW(on)}$:	IGBT's turn-on switching energy per pulse at peak current, I_{CP} and T = 125°C
$E_{SW(off)}$:	IGBT's turn-off switching energy per pulse at peak current, I_{CP} and T = 125°C
f_{SW}:	PWM switching frequency for every inverter arm-switch (normally, $f_{SW} = f_C$)
I_{CP}:	Peak value of sinusoidal output current ($I_{CP} = I_{EP}$)
$V_{CE}(SAT)$:	IGBT saturation voltage drop @I_{CP} and T = 125°C
V_{EC}:	FWD forward voltage drop @ I_{EP} (refer Powerex data)
D:	PWM duty factor (modulation depth)
θ:	Phase angle between output voltage and current
I_{RR}:	Diode peak recovery current
t_{RR}:	Diode reverse recovery time
$V_{CE}(pk)$:	Peak voltage across the diode at recovery

Figure 3.10 Typical VVVF Inverter Circuit and Output Waveform



3.4.3 Loss Estimation by Calibrated Heatsink Method

In many applications it is difficult to make the precision measurements of voltage and current that are necessary to accurately calculate switching losses. It can also be difficult to make these measurements without disturbing low inductance power circuits to the point of making the accuracy suspect. In some cases the operating voltage, gate resistance, drive voltage, power circuit configuration or snubber design is significantly different from standard conditions making use of published switching energy data impossible. For all of the above cases the following alternate method of power loss estimation should be used:

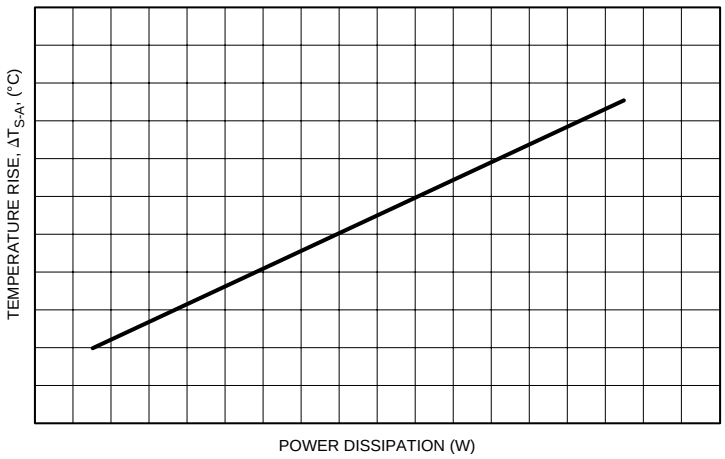
(1) Mount IGBT module in the thermal system (fan, heatsink, cabinet etc.) exactly as it will be used in the final design.
(2) Bias device on by applying isolated +15V DC power to the gate emitter or in the case of IPM apply control power and pull the control input signal low.
(3) Connect the IGBT to a low voltage current regulated DC power supply and operate at several different DC currents gradually increasing until the current is approximately equal to the expected average operating current. Be careful not to exceed the IGBT junction temperature ratings while performing this test.
(4) For each test current allow the system to reach thermal equilibrium and record the temperature rise of the heat sink above ambient temperature near the IGBT module. At the same time, using an accurate DMM measure and record the voltage drop across the IGBT and the DC current. Power dissipation in the IGBT can be easily calculated by multiplying the DC current by the voltage drop across the device.

The data gathered in the above test can be used to make a thermal system calibration curve like the one shown in Figure 3.11. Now, when the IGBT is operated normally the total power dissipation including both switching and conduction components can be determined simply by measuring the heat sink temperature rise and reading from the calibration curve. This technique for loss estimation is very effective for estimating operating junction temperature. The power determined from the curve can be multiplied by the devices thermal impedances as outlined in Section 3.4.4 to determine the junction temperature. Even in cases where published loss curves can be used this method of loss estimation is often a valuable tool for refining the thermal system design.

3.4.4 Estimating Average Junction Temperature

The IGBT chips in the Power Module have a maximum rated junction temperature of 150°C. This rating should not be exceeded under any normal operating condition. Good design practice is to limit the worst case maximum junction temperature to 125°C or less. Reliability can be enhanced by operating the semiconductor junction at lower temperatures. If the total average power dissipated in the semiconductor device and the module base plate temperature are known, the junction temperature can be estimated using thermal resistance concepts as shown in Figure 3.12. Thermal resistance (R_{th}) is specified on the

Figure 3.11 Typical Heat Sink Calibration Curve



Power Module data sheet for use in thermal calculations. Junction temperature is estimated using the following equation.

$T_j = T_C + P_T \times R_{th(j-c)}$

Where:

$R_{th(j-c)}$ = Specified junction to case thermal resistance
T_j = Semiconductor junction temperature
P_T = Total average power dissipated in device ($P_{SW} + P_{cond}$)
T_C = Module base plate temperature

By using the appropriate values of $R_{th(j-c)}$ and P_T the above equation can be used to estimate the junction temperature of either the IGBT or the free-wheel diode.

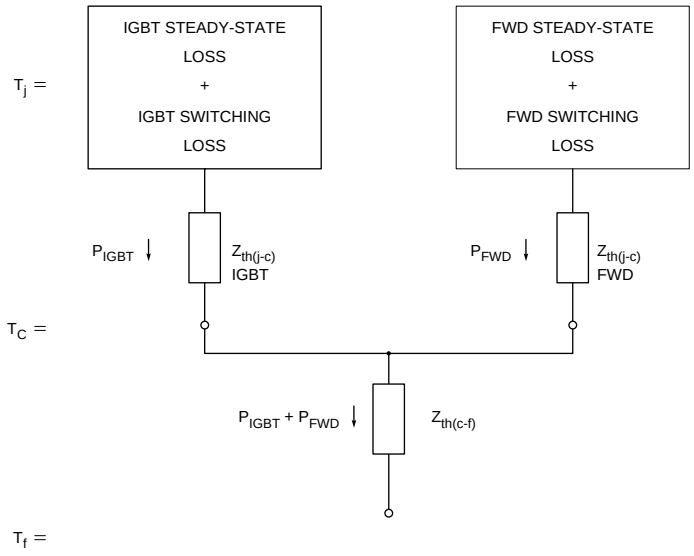
For initial design of heat sink systems, contact thermal resistance is specified on the Power Module data sheet. Contact thermal resistance is the thermal resistance of the module to heat sink interface. The specified value assumes that a thermal interface compound such as white grease is used. A uniform layer of non-volatile silicon thermal grease with a nominal thickness of approximately 6 mills will give the best results. The module base plate temperature can be estimated using the following equation.

$T_C = T_a + P_T \times (R_{th(c-f)} + R_{th(f-a)})$

Where:

P_T = Total power dissipated in an IGBT FWD pair.
$R_{th(c-f)}$ = The interface thermal resistance.

Figure 3.12 Thermal Calculation Model



$R_{th(f-a)}$ = The heat sink to ambient thermal resistance specified by the heat sink manufacturer.
T_a = Ambient temperature

The value of $R_{th(c-f)}$ is specified for the entire module. Final thermal analysis should be done using measured base plate temperature and total power loss under worst case conditions.

3.4.5 Estimating Junction Temperature Rise

For short or low duty cycle power pulses, using the steady state thermal resistance will give conservative junction temperatures. In addition, using the average value of power dissipation will underestimate the peak junction temperature. The solution is use of the transient thermal impedance curves. Figure 3.13 illustrates typical transient thermal impedance curves. For a power device subjected to a single or very low duty cycle, short duration power pulses, the maximum allowable power dissipation during the transient period can be substantially greater than the steady state dissipation capability.

Calculation of the peak transient junction temperature rise depends on the duty factor and repetition rate of the power pulses. Figure 3.14 describes the application of the transient thermal impedance curve to a variety of power pulse situations. Please consult Powerex Application Engineering for guidance in the use of the equations contained in this figure as well as their application to irregular and overload power pulses.

3.4.6 Heatsink Mounting

When mounting IGBT modules on a heatsink avoid uneven mounting stress. Heatsink flatness requirements are shown in Figure 3.15. Avoid one sided tightening stress. Figure 3.18 shows the recommended torque order for mounting screws. Uneven mounting can cause the modules ceramic isolation to crack.

Do not over torque terminal or mounting screws. Maximum torque specifications are provided in device data sheets. Mounting screws should be tightened to the prescribed torque in progressive stages in a cross pattern to prevent unbalanced tightening, uneven contact, or mechanical bending stress.

(A) Use a torque wrench to tighten the screws in the prescribed cross pattern.

(B) Tighten the screws first with just enough torque to bring the screw head into contact with the device, then to 50% of the prescribed maximum value, and finally to 90 to 100% of the prescribed maximum torque.

The heatsink should have a surface finish of 64 microinches or less. Use a uniform 4 to 8 mil coating of thermal interface compound. Select a compound which has stable characteristics over the whole operating temperature range and does not change its properties over the life of the equipment. See Table 3.2 for suggested types.

Table 3.2 Heatsink Compounds

Manufacturer	Type
Shinetsu Silicon	G746
Dow Corning	DC340

3.4.7 Power Cycling Considerations

A final thermal design consideration is the temperature range, ΔT_j, through which the junction will cycle as the equipment operates in actual application. The concern here is what is called thermal fatigue. That is, as the component parts of the module heat and cool due to collector power dissipation there are mechanical stresses caused by the different coefficients of expansion of the various component materials. This differential expansion puts the intermediate layers under bending and shear stress. With the accumulation of these stress cycles the assembly structure can deteriorate causing eventual failure. Studies of this phenomenon involve tests at multiple operating points to create curves that indicate cycling life as a

Figure 3.13 Transient Thermal Impedance Curves

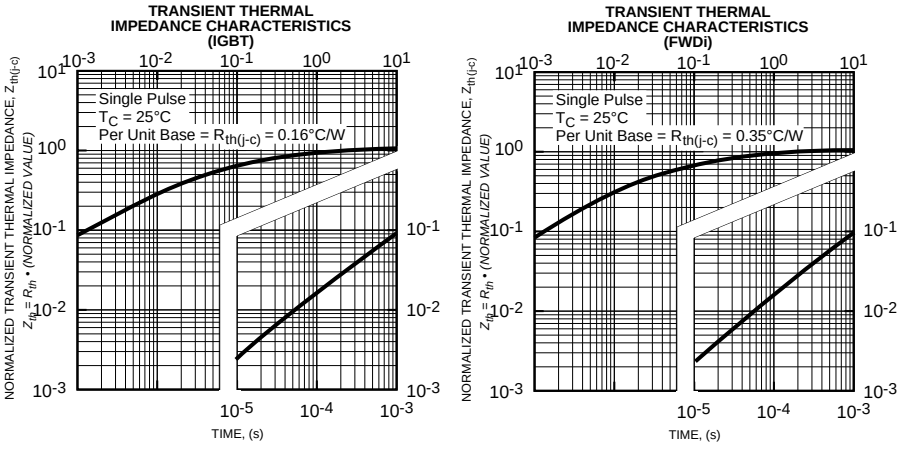
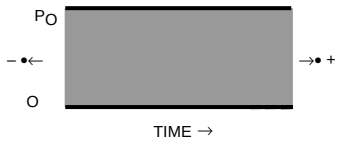
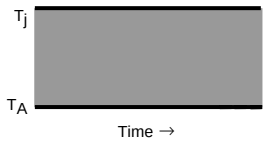
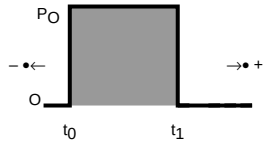
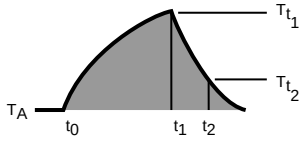
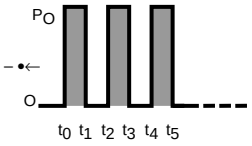
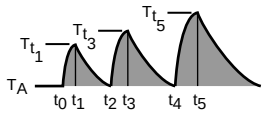
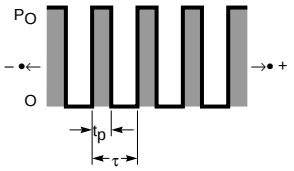
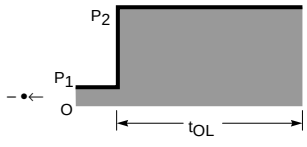
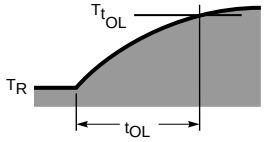
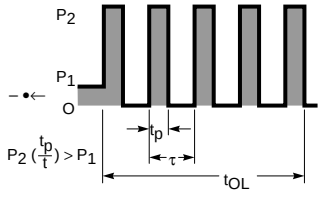
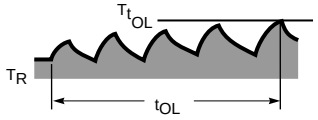


Figure 3.14 Junction Temperature Calculations Using Transient Thermal Impedance

Load Condition	Waveform of Power Loss at Junction	Solution for Juction Temperature θ = Steady-State Thermal Resistance θ (t_1) = Transient Thermal Impedance at Time T_1 θ ($t_2 - t_1$) = Transient Thermal Impedance at Time ($t_2 - t_1$), etc.	Waveform of Junction Temperature Rise (T_A = Reference Temp.)
Continuous Load		$T_j - T_A = P_O\theta$	
Single Load Pulse		$T_{t_1} - T_A = P_O\theta(t_1)$ $T_{t_2} - T_A = P_O[\theta(t_2) - \theta(t_2 - t_1)]$	
Short Train of Load Pulses (Equal Amplitude)		$T_{t_1} - T_A = P_O\theta(t_1)$ $T_{t_3} - T_A = P_O[\theta(t_3) - \theta(t_3 - t_1)] + \theta(t_3 - t_2)]$ $T_{t_5} - T_A = P_O[\theta(t_5) - \theta(t_5 - t_1)] + \theta(t_5 - t_2)]$, etc.	
Long Train of Equal Amplitude Load Pulses (Approx. Solution)		$T_j - T_A = P_O[\frac{t_p\theta}{\tau} + (1 - \frac{t_p}{\tau})\theta(\tau + t_p) - \theta(\tau) + \theta(t_p)]$	
Overload Following Continuous Duty (Non-Pulsed)		$T_{t_{OL}} - T_A = P_1\theta + (P_2 - P_1)\theta(t_{OL})$	
Overload Following Continuous Duty (Pulsed) (Approx. Solution)		$T_{t_{OL}} - T_A = P_1\theta + P_2\left\{\left[\frac{t_p}{\tau} - \frac{P_1}{P_2}\right]\theta(t_{OL})\right.$ $\left. + (1 - \frac{t_p}{\tau})\theta(\tau + t_p) - \theta(\tau) + \theta(t_p)\right\}$	

function of the ΔT_j excursion. These curves are specific to particular temperature, time, and operating ranges, so that a general curve cannot be generated and published. The curve in Figure 3.16 is representative of the worst case test result for ALN ceramic isolated modules. Experimental studies have shown that a relatively long heating and cooling cycle of the order of two minutes that causes the base plate temperature of the module to change along with the junction temperature is usually the worst case. The curve in Figure 3.16 should not be confused with the commonly published "power cycle" curves that are derived using a short heating cycle of 10 seconds or less. Under such short cycle conditions Powerex modules can be expected to have five to ten times the life indicated in Figure 3.16.
Figure 3.16 is an example curve taken for modules using the test setup shown in Figure 3.17. All available information has indicated that thermal fatigue is not an issue when ΔT_j is kept below 30°C. For applications involving a large number of power cycles in conjunction with junction temperature excursions greater than 30°C the application should be reviewed in detail with Powerex Application Engineers.

Figure 3.15

HEAT SINK FLATNESS REQUIREMENTS

MODULE BASE PLATE MATERIAL	HEAT SINK FLATNESS
COPPER TYPE MODULE	-100μm ~ +100μm
ALUMINUM TYPE MODULE	-50μm ~ +100μm

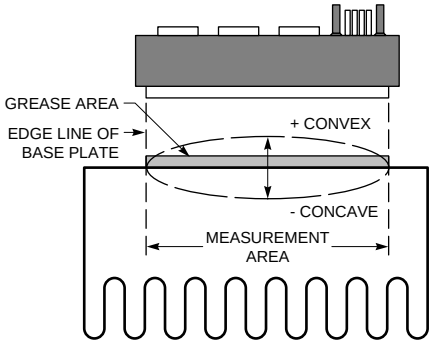


Figure 3.16 Intermittent Operation Life Curve

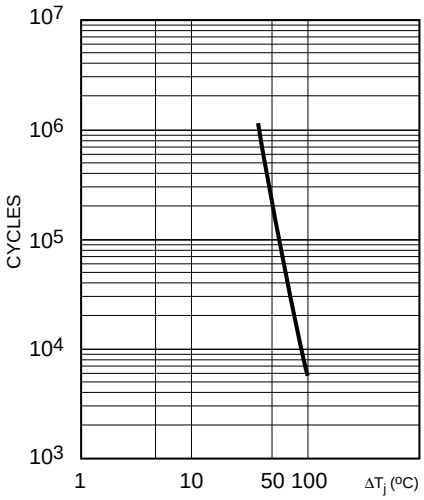
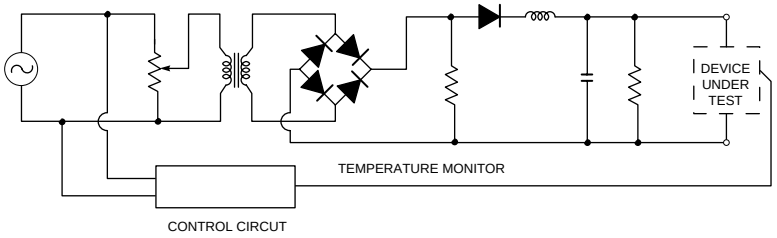


Figure 3.17 The Power-cycle Test Circuit



3.5 Reliability

High reliability standards are assured with Powerex semiconductor devices through the rigorous quality control inspections which the devices are subjected to in the design and manufacturing stages. The quality assurance inspections run on each production lot and numerous reliability tests have been implemented in order to maintain this standard of reliability.

Table 3.3 shows the result of reliability tests of a typical IGBT Module. Figure 3.19 shows the results of several reliability tests illustrating the typical changes as a function of time. Table 3.4 shows the failure criteria.

3.5.1 Test Results

Following are the results of semiconductor reliability tests on a typical IGBT Module.

SEMICONDUCTOR RELIABILITY TESTS

Semiconductor reliability tests are intended to simulate or accelerate all the possible stresses that semiconductor devices might be subjected to at the various phases of its life, including mounting on equipment, performance, aging, and field installation and operation. They are composed of environmental tests and separate endurance tests. Each set of test conditions and results are shown in Table 3.3, and time dependent characteristics of some test items are shown in Figure 3.19.

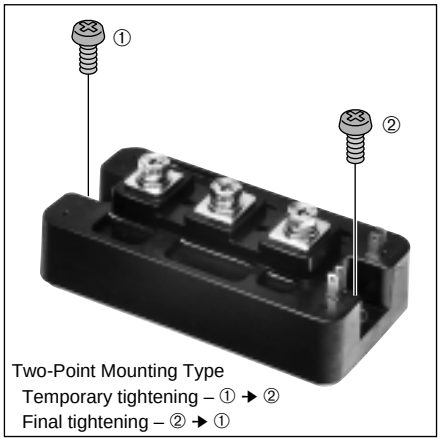
FAILURE CRITERIA

Failure criteria are shown in Table 3.4. The characteristics of a failed device are verified based on these criteria and the device status (good or bad) is determined. Before measurement, each device is kept at room temperature for two hours. After performing such tests as temperature humidity test, in which water is used, the devices are dried at 125°C for 2 hours before measurement.

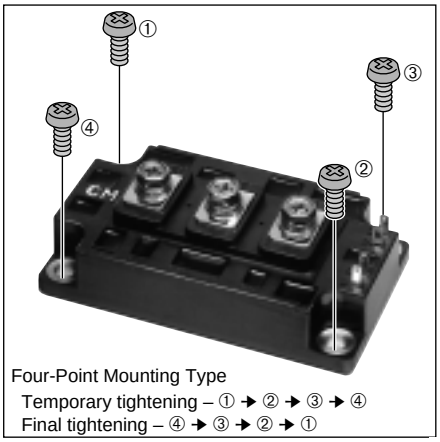
RESULTS

Results of each test performed on the above mentioned IGBT modules are satisfactory. The reliability aspects of the module are confirmed as determined in the following pages.

Figure 3.18 Recommended Torquing Order for Mounting Screws



Two-Point Mounting Type
Temporary tightening – ① → ②
Final tightening – ② → ①



Four-Point Mounting Type
Temporary tightening – ① → ② → ③ → ④
Final tightening – ④ → ③ → ② → ①

Table 3.3 Reliability Test Results

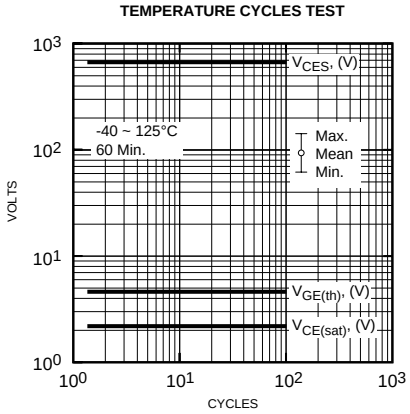
Test Category	Test Conditions	Conforms to JIS C 7021	Sample Size	Number of Failures	Remarks
Temperature Cycling	-40 ~ 125°C 60 minutes each 100 Cycles	A-4	5	0	See Figure 3.18 (A)
Thermal Shock	0 ~ 100°C 5 minutes 100 Cycles	A-3	5	0	
Free Fall	Dropping from the height of 75CM wooden board, 3 times	A-8	5	0	
Variable Frequency Vibration	10 ~ 500 HZ/15 minutes 10G XYZ 2 hours each	A-10	5	0	
Terminal Strength	4.5kg 30 seconds	A-10	5	0	
Tightening Strength	M6: 30kg/cm M5: 20kg/cm	A-10	5	0	
High Temperature Life	T_a = 125°C 1,000 hours	A-10	5	0	
Low Temperature Life	T_a = 40°C 1,000 hours	A-10	5	0	
Moisture Resistance	T_a = 60°C, 90% RH 1,000 hours	A-10	5	0	See Figure 3.18 (B)
High Temperature Reverse Bias	T_a = 125°C V_{CE} = 510V, V_{GE} = 0V 1,000 hours	A-10	5	0	See Figure 3.18 (C)
High Temperature Gate Bias	T_a = 125°C V_{GE} = 20V, V_{CE} = 0V 1,000 hours	A-10	5	0	See Figure 3.18 (D)
Intermittent Operation Life	I_C = 50A T_C = 50 ~ 80°C On-time: 53 seconds Off-time: 62 seconds 10,000 cycles	B-6	5	0 Figure	See 3.18 (E)

Table 3.4 Failure Criteria for the Reliability Test

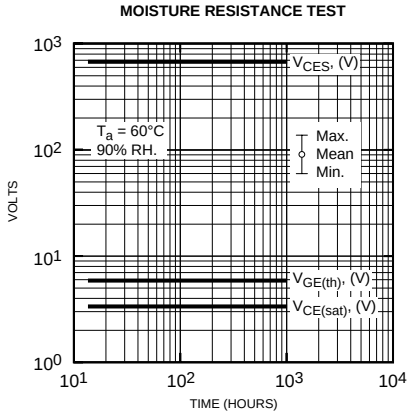
Parameter	Test Conditions	Criteria for Failure	Remarks
V_{CES}	I_C = 1mA, V_{GE} = 0V	Rating x 0.8	
I_{CES}	V_{CE} = 600V, V_{GE} = 0V	Rating x 2.0	
I_{GES}	V_{GE} = ±20V, V_{CE} = 0V	Rating x 2.0	
$V_{GE(th)}$	I_C = 10mA, V_{CE} = 10V	Rating x 1.2 Rating x 0.8	
V_{CE}(SAT)	I_C = 100A, V_{GE} = 15V	Rating x 1.2	
V_{EC}	I_E = 100A	Rating x 1.2	
Dielectric Withstand	AC 2500V, 1 minute	Breakdown	

Figure 3.19 The Results of Reliability Test of a 600V/100A IGBT Module

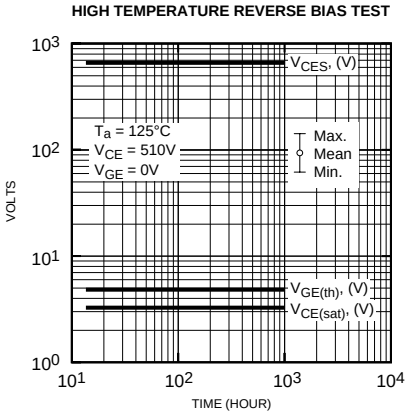
(A) Temperature Cycles Test (-40 ~ 125°C, 60 minutes)



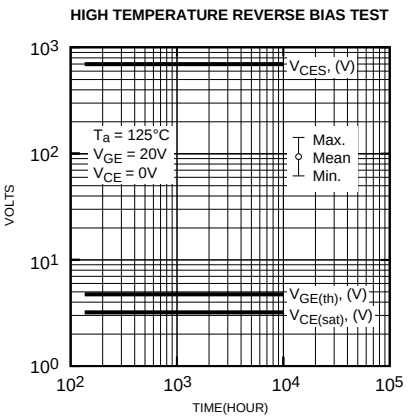
(B) Moisture Resistance Test (T_a = 60°C, 90% RH)



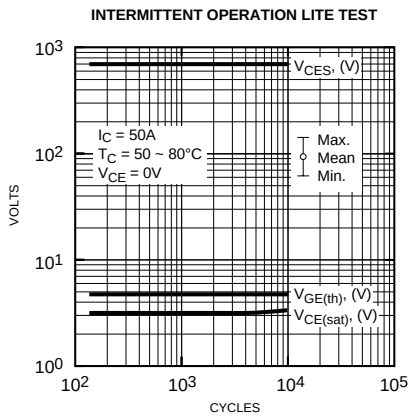
(C) High Temperature Reverse Bias Test (T_a = 60°C, V_{CE} = 510, V_{GE} = 0V)



(D) High Temperature Gate Bias Test (T_a = 125°C, V_{CE} = 510V, V_{GE} = 0V)



(E) Intermittent Operation Life Test (I_C = 50A, T_C = 50 ~ 80°C)



NOTE:

Sample: 600V/100A IGBT Module
: 5 pieces

Parameter Condition

V_{CES} : at I_C = 1mA, V_{GE} = 0V
$V_{CE(sat)}$: at I_C = 100A, V_{GE} = 15V
$V_{GE(th)}$: at I_C = 10mA, V_{CE} = 10V