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4.0 Using IGBT Modules

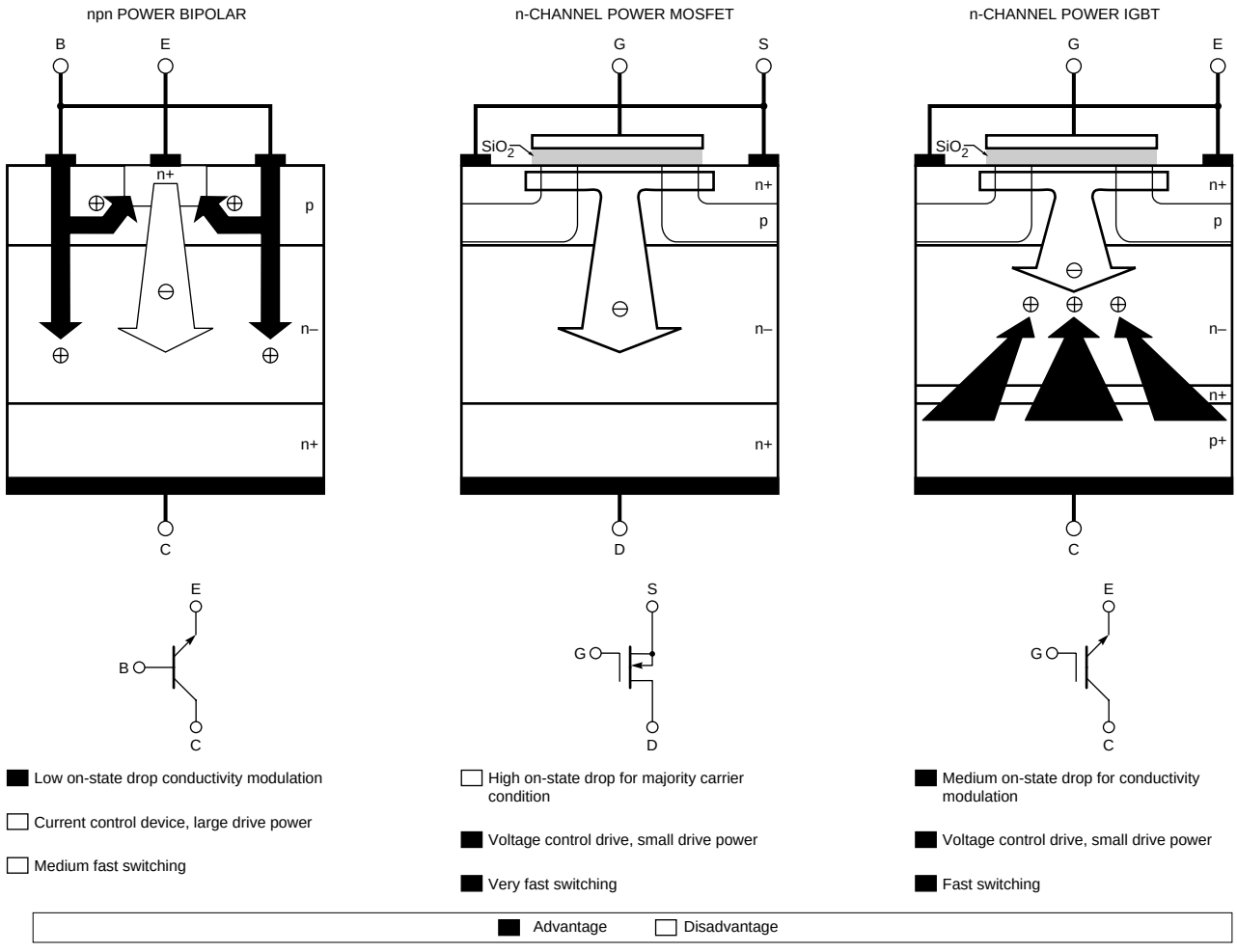
Powerex IGBT modules are designed to be rugged, low loss and easy to use. Use of advanced processing technologies gives low on-state saturation voltages while maintaining the high switching speed needed for 20kHz operation. The information presented in this section is intended to help users of Powerex IGBT modules apply the devices effectively and reliably.

4.1 Structure and Operation of IGBT Module

The IGBT, Insulated Gate Bipolar Transistor, is a switching transistor that is controlled by voltage applied to the gate terminal. Device operation and structure are similar to those of an Insulated Gate Field Effect Transistor, more commonly known as a MOSFET. The principal difference between the two device types is that the IGBT uses conductivity modulation to reduce on-state conduction losses.

A brief comparison between the structures of the IGBT, MOSFET and npn Bipolar Junction Transistor (BJT) is depicted in Figure 4.1. The npn BJT is a three junction device that requires a continuous current flowing into the base region to supply enough charges to allow the junctions to conduct current. Because the MOSFET and the IGBT are voltage controlled devices, they only require voltage on the gate to maintain conduction through the device. The IGBT has one junction more than the MOSFET, and this

Figure 4.1 Three Major Device Technologies



junction allows higher blocking voltage and conductivity modulation, as described below, during conduction. This additional junction in the IGBT does limit switching frequency however.

4.1.1 Silicon Structure

The IGBT silicon structure is as shown in Figure 4.2. A positive voltage on the gate attracts electrons from the “p” gate region towards the silicon surface under the gate. These electrons invert the “p” directly under the gate to form an “n” region, thus creating a path for charge flow between the “n” collector region and the “n” emitter region. A zero or negative voltage (depends on the device) on the gate maintains the off-bias.

4.1.2 Device Operation

When the device is on, the collector is at a higher voltage than the emitter, and therefore minority carriers are injected from the collector p+ region into the collector bulk region (n+ buffer layer and collector “n” region). The charges reduce the collector bulk region resistance and thus collector to emitter voltage drop is reduced (relative to $V_{DS(on)}$ of MOSFET).

When a positive gate voltage is first applied, a gate current flows until the gate capacitance is charged and the gate voltage rises to the “on” level. When the gate voltage is removed, the charges injected into the collector bulk region must be removed before high voltage can be blocked.

The IGBT surface emitter pattern is striped geometrically, in contrast to the FET cell-based geometry. The IGBT uses the same small feature size advantages of the MOSFET, but the striped geometry offers more ruggedness and immunity from latch-up of the parasitic thyristor shown in Figure 4.3A.

A circuit model of a typical IGBT is illustrated in Figure 4.3A. Powerex IGBTs use optimized buffer layer, p± well doping and alignments, gate structure, and surface pattern designs. Minority carrier lifetime control techniques are used to reduce the gain of the “pnp” bipolar element and minimize lateral R_{BE} values, thus precluding latch-up. Therefore, the equivalent circuit model of a Powerex IGBT is reduced to the schematic in Figure 4.3B.

4.1.3 Wafer Processing

IGBT wafer processing is similar to FET processing. The silicon material is a dual epitaxial structure, and gate and emitter regions are diffused and/or ion implanted into the emitter side. Selective doping, electronic irradiation, and other processing techniques are used during emitter-side processing.

Many of the same processing techniques used to fabricate FET devices are employed in IGBT manufacture. The high di/dt and dv/dt capabilities of the FETs result from the control of minority carriers near the gate “p” region and collector “n” region interface. The same techniques plus additional steps to control carrier lifetime near the collector N+ buffer region help to generate immunity from latch-up and to enhance the

Figure 4.2 IGBT Cross Section and Silicon Structure

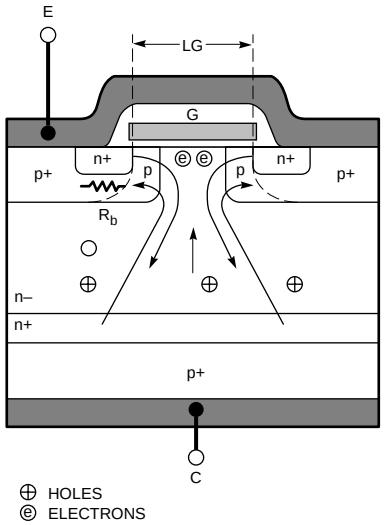
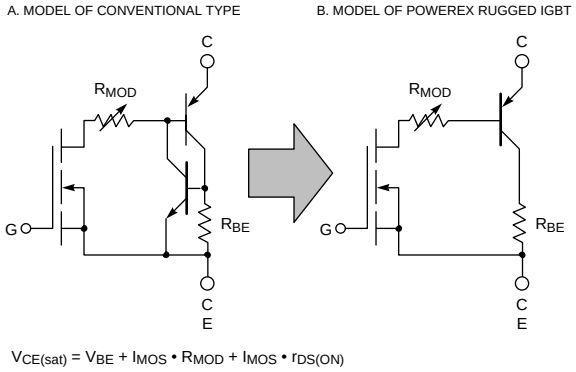


Figure 4.3 IGBT Internal Parasitics



$V_{CE(sat)} = V_{BE} + I_{MOS} \bullet R_{MOD} + I_{MOS} \bullet r_{DS(ON)}$

Figure 4.4 Structure of Powerex IGBT Module and Module Base Plate Construction

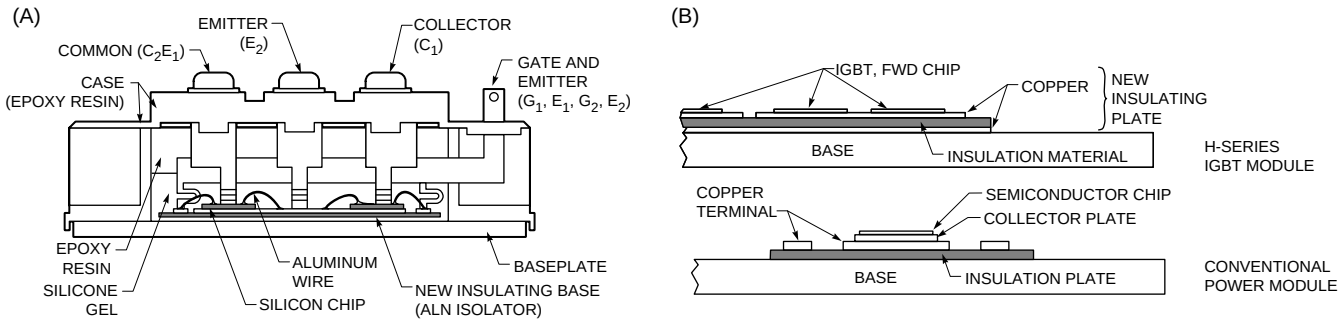
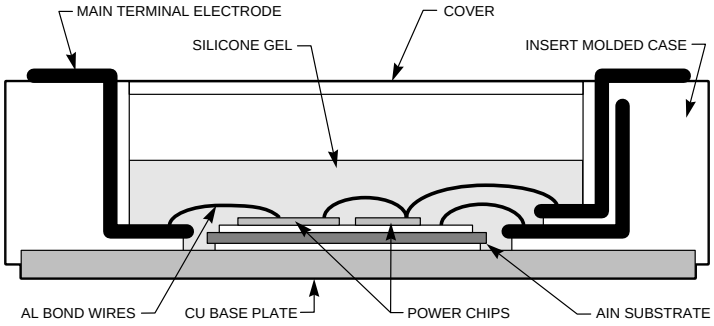


Figure 4.5 Cross Section of U-Package IGBT Module



switching ruggedness of Powerex IGBTs. Ultra clean facilities and in-line wafer testing promote consistent processing, thus ensuring chips of the highest quality and reliability.

4.1.4 Module Packaging Construction and Layout

IGBT modules consist of multiple IGBT chips mounted on an isolated substrate, which is itself mounted on a heatsinking copper base plate as shown in Figure 4.4A.

Powerex IGBT modules use an isolating ceramic substrate with copper patterns metallurgicly bonded to the top and bottom surfaces. (Figure 4.4B). This mounting method allows highly automated module assembly while minimizing thermal impedance. Powerex IGBT modules use materials with similar thermal coefficients of expansion so that thermal stress is limited. Thus these IGBT modules can be expected to provide improved thermal cycle life over existing power transistor modules.

Free-wheeling diodes are also mounted in the module for ease of system assembly and to allow minimum lead inductance, both inside and outside the module. Interconnection inside the modules is accomplished with rigid bussing to ease assembly. Rigid bussing also offers symmetric layout of internal components so the parasitic inductance is reduced and module ruggedness is enhanced.

4.1.5 Features of U-Package IGBT Modules

A new IGBT module package called “U-Package” was developed by Mitsubishi Electric in alliance with Powerex in 1996. The new package technology achieves a significant reduction in internal inductance and improved reliability over older designs. The time required to assemble the new module was substantially reduced by using a special case that has the power electrodes molded into its sides rather than inserted after the case is molded. Figure 4.5 is a cross section drawing of the new IGBT module package. The main electrodes are connected directly to the power chips using large diameter aluminum bonding wires. In order to help simplify power circuit and snubber designs or possibly eliminate the need for snubbers altogether an effort was made to minimize the inductance of the new U-Package. A variety of techniques were used to reduce each component of the package inductance. One of the most significant improvements was made possible by the new insert molded case design. Wide electrodes are molded into the side of the case to form parallel plate

structures that have considerably less inductance than conventional electrodes. In addition, the strain relieving “S” bends that were needed in the electrodes of conventional modules are not needed in the U-Package because the aluminum bond wires perform the strain relieving function. Elimination of these “S” bends helped to further reduce the electrode inductance. Overall, as a result of these inductance reducing features the U-Package modules typically have about one third the inductance of conventional modules. A further reduction in assembly time was achieved by reducing the number of soldering steps during manufacturing. With the conventional module the chip to substrate and substrate to base plate soldering is done first with high temperature solder. Then the case is attached to the base plate and a second low temperature soldering step is used to connect the power electrodes. In the new module the second step is not needed because the connections to the power electrodes are made using the aluminum bond wires. The soldering temperature of the chip and substrate attachment can be reduced. The lower soldering temperature minimizes the effects of the mismatched coefficients of expansion between the base plate and the AlN DBC substrate. The result is a reduction in thermal stress during manufacturing and improved power cycle reliability.

4.2 IGBT Module Ratings and Characteristics

The ratings as shown in Section 4.2 are most important for IGBT's operation and environment. A maximum rating is a value which establishes either a limiting capability or limiting condition (either maximum or minimum). It is determined for a specified value of environment and operation. Therefore, you cannot use the IGBT module beyond its maximum or minimum rating's value.

4.2.1 Absolute Maximum Ratings

Symbol	Parameter	Definition
V_{CES}	Collector-Emitter Blocking Voltage	Maximum off-state collector-emitter voltage with gate-emitter shorted
V_{GES}	Gate-Emitter Voltage	Maximum gate-emitter voltage with collector-emitter shorted
I_C	Continuous Collector Current	Maximum collector current
I_{CM}	Peak Collector Current Repetitive	Peak collector current, $T_j \leq 150°C$
I_E	Continuous Diode Current	Maximum diode current
I_{EM}	Peak Diode Current Repetitive	Diode peak current, $T_j \leq 150°C$
P_D	Power Dissipation	Maximum power dissipation, per device, $T_C = 25°C$
T_j	Junction Temperature	Allowable range of IGBT junction temperature during operation
V_{ISO}	Isolation Voltage	Minimum RMS isolation voltage capability applied electric terminal to base plate, 1 minute duration
	Mounting Torque	Allowable tightening torque for terminal and mounting screws

4.2.2 Electrical Characteristics

Symbol	Parameter	Definition
Static		
I_{CES}	Collector-Emitter Leakage Current	I_C at $V_{CE} = V_{CES}$, $V_{GE} = 0$, gate-emitter shorted, $T_j = 25°C$
I_{GES}	Gate-Emitter Leakage Current	I_G at $V_{GE} = V_{GES}$, $V_{CE} = 0$, collector-emitter shorted, $T_j = 25°C$
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	V_{GE} at I_C = specified mA, $V_{CE} = 10V$
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_{CE} at I_C = rated I_C and $V_{GE} = 15V$
Q_G	Total Gate Charge	Charge on gate at V_{CC} - 0.5~0.6V_{CES}, rated, I_C = rated I_C, $V_{GE} = 15V$
V_{FM}	Diode Forward Voltage	Diode voltage at I_C = -rated I_C, $V_{GS} = 0V$
Dynamic		
C_{ies}	Input Capacitance	Gate-emitter capacitance with the collector shorted to the emitter
C_{oes}	Output Capacitance	Collector-emitter capacitance with the gate shorted to the emitter
C_{res}	Reverse Transfer Capacitance	Gate-collector capacitance with the emitter connected to the guard terminal of the impedance analyzer

4.2.2 Electrical Characteristics (Continued)

Symbol	Parameter	Definition
Dynamic (Continued)		
$lt_{d(on)}$	Turn-on Delay Time	Time from V_{GE} = 0V to I_C = 10% of final value
t_r	Rise Time	Time from I_C = 10% of final value to I_C = 90% of final value
$t_{d(off)}$	Turn-off Delay Time	Time from V_{GE} = 90% of initial value to I_C = 90% of initial value
t_f	Fall Time	Time from I_C = 90% of initial value to I_C = 10% of initial value
t_{rr}	Diode Reverse Recovery Time	Time from I_C = 0A to projection of zero I_C from I_{rr} and 0.5 I_{rr} points with I_C = -rated I_C and at specified di/dt (Refer to Figure 4.6)
Q_{rr}	Diode Reverse Recovery Charge	Area under I_{rr} curve from I_C = 0A to projection of zero I_C from I_{rr} and 0.5x I_{rr} points with I_C = rated I_C and at specified di/dt (Refer to Figure 4.6)

4.2.3 Thermal Characteristics

Symbol	Parameter	Definition
$R_{th(j-c)}$	Thermal Resistance, Junction to Case	$(T_j - T_C)/(I_C\text{-X } V_{CE})$, I_C conducting to establish thermal equilibrium
$R_{th(c-f)}$	Thermal Resistance, Case to fin	$(T_C - T_f)/(I_C \text{ X } V_{CE})$, I_C conducting to establish thermal equilibrium lubricated

Figure 4.6 Reverse Recovery Measurement Circuit and Waveform

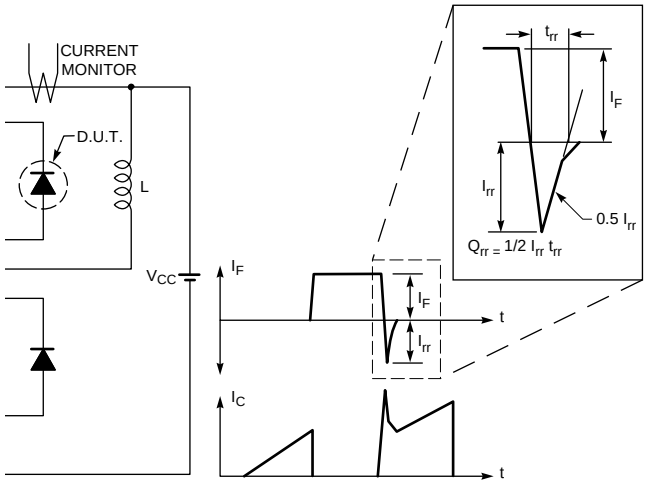


Figure 4.7 V_{CE} (SAT) Test

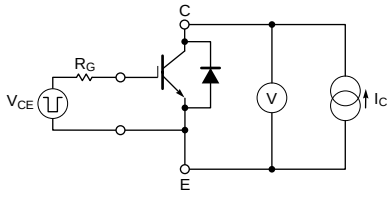
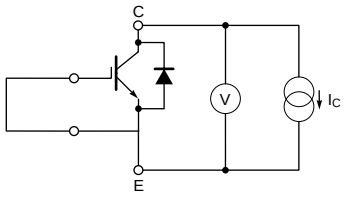


Figure 4.8 V_{CE} Test



4.2.4 Test Circuits and Conditions

The following test circuits are used to evaluate IGBT characteristics.

1. V_{CE}(SAT) and V_{EC}
   To ensure specified junction temperature, T_j, measurements of V_{CE} (SAT) and V_{EC} must be performed as low duty factor pulsed tests. (See Figures 4.7 and 4.8)
2. Resistive Load Switching Test Circuit. (See Figure 4.9)
3. Half-Bridge Switching Test Circuit (See Figure 4.10)

Figure 4.9 Resistive Load Switching Test Circuit

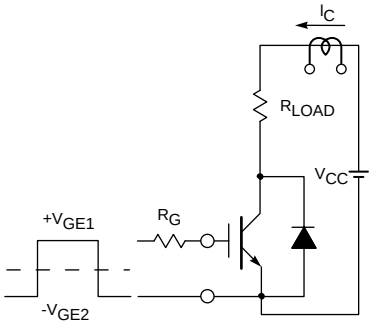


Figure 4.10 Switching Time Waveform

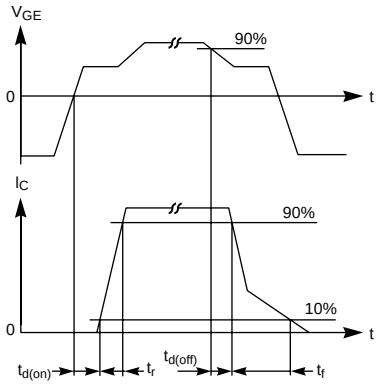
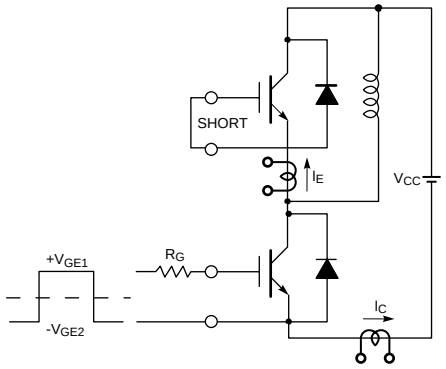


Figure 4.11 Half-bridge Switching Test Circuit



4.3 Safe Operation Area

Protecting IGBTs against disturbance caused by over currents or over voltage is an important design topic in most switching applications. In the case of all hard switching applications, such as inverter or chopper circuits for motor controls and transformer loads, the turn-off switching SOA and short circuit capability are the two most important ratings of IGBTs today.

4.3.1 The Turn-off Switching SOA of IGBT

The turn-off switching SOA is similar to RB SOA (Reverse Bias SOA) of Darlington transistors. The switching operation for a typical inverter bridge circuit as shown in Figure 4.11, will generate the current and voltage waveform illustrated in Figure 4.12. In turning off an inductive load current, the voltage rise precedes the current fall. As the gate voltage reduces below its threshold value, the intrastructural MOSFET channel window gets blocked and injection of electrons cease. Removal of the stored minority carriers (holes) in the "n" base region starts, and during this interval, the parasitic wide base pnp transistor operated by virtue of its current gain characteristics causing the collector current to continue flowing. Thus, the later part of the IGBT turn-off fall current, is mainly due to the hole current. Some of the holes in the "n" base region continues to cross through the C-B junction of the parasitic npn transistor and travel horizontally below the "n" emitter layer as shown in Figure 4.13.

This flow of holes causes a potential drop across the "p" body resistance, R_D, and tends to activate the npn transistor. A turn on of the npn transistor, while the pnp transistor is still active, can lead to pnp thyristor latch-up, which means loss of gate control and, eventually, destruction of the device. This problem has been eliminated in the Powerex IGBTs by careful optimization of the device geometry.

The switching SOA curve is the locus of points defining the maximum allowable simultaneous occurrence of collector current and collector to emitter voltage during turn-off. Figure 4.14 shows that Powerex IGBTs offer square switching SOA for 600V and 1200V devices at 2X rated current.

The curves show that independent of V_{CE}, the device current must be kept below 200% rated current. This limit is due to the designed current density of the chips and internal connections in the module.

4.3.2 Short Circuit SOA

Most power conversion applications require that the applied switch should survive a short circuit on the system output without any damage. When considering short circuit withstand capability of IGBT

Figure 4.12 Switching Waveforms (Half-bridge Mode)

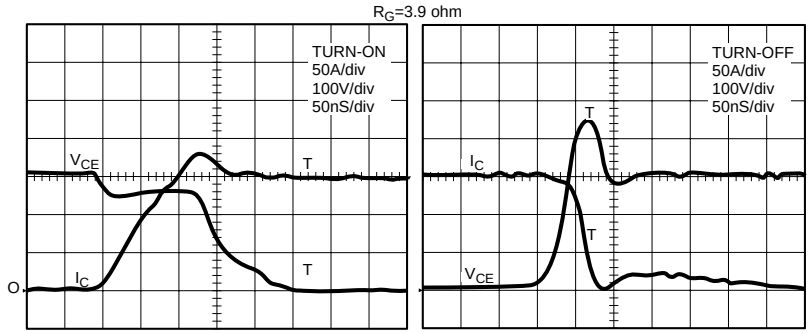


Figure 4.13 High Injection On-state Electron and Hole Currents within an IGBT Structure

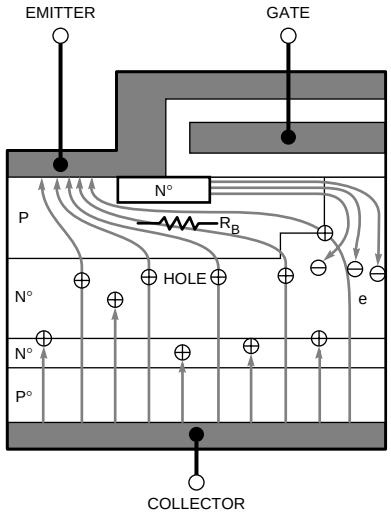
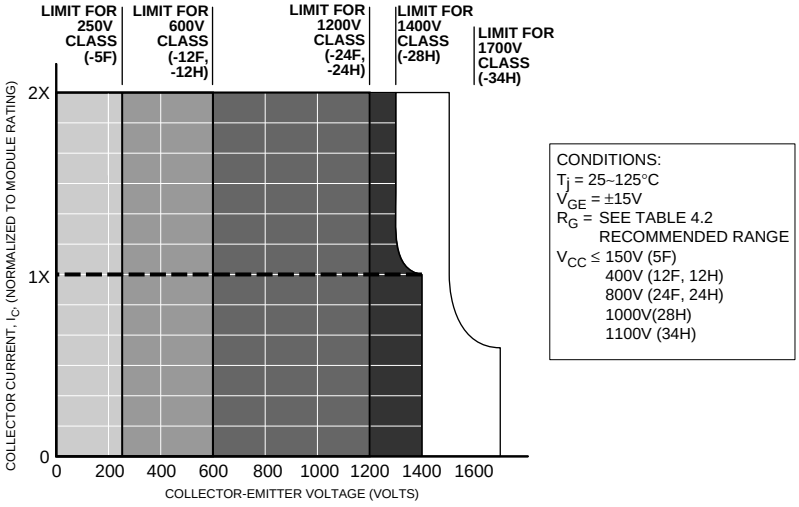


Figure 4.14 Turn-off Switching SOA



modules, two distinguishing cases are generally reviewed:

Case-1 – Switching on of an IGBT into a short circuit,

Case-2 – Load or groundfault short circuit across a switched on IGBT.

Figure 4.15 shows the circuitry and waveforms for each case.

In Case-1, as the IGBT turns on, initial rate of rise of I_C is determined by the wiring inductance, L. Also, the voltage, V_{CE}, drops to some value below V_{CC} as the L discharges. Soon after this, V_{CE} switches back to almost full V_{CC} level. The dv/dt at this switch back is coupled to the gate through the reverse transfer capacitance thus causing a momentary rise of gate voltage.This extra gate voltage mobilizes more electron and hole plasma within the IGBT module structure. The effect of this translates to a higher peak collector current within a couple of microseconds. The circuit design (e.g. layout, bias condition, selection of R_g, maximum supply voltage, etc.) is important to limit the short circuit current magnitude in this high injection state. Due to high current density within the silicon, the internal temperature rises and it causes the high short circuit peak current to reduce to a lower value which corresponds to what is called a saturation current. To protect the device from destruction, the current has to be cut off within a specified period, which is normally specified by the input gate pulse width, t_w. At turn-off, a sharp fall of collector current in the presence of the wiring inductance, L_1, causes

V_{CE} to shoot up by an amount equivalent to:

$$\Delta V_{CE} \approx L_1 \text{ X } di_C/dt.$$

The instantaneous value of collector-emitter voltage, V_{CE}, including this surge peak value must not be allowed to go beyond the specified voltage limit given by SCSOA as shown in Figures 4.16, 4.17, 4.18, 4.19, and 4.20.

In Case-2 short circuit an external short circuit occurs while the IGBT is already in the on state. as shown in Figure 4.15B) The increasing short circuit forces the IGBT chip to desaturate causing the collector-emitter voltage to rise from V_{CE}(SAT) to almost full V_{CC}. The dv/dt during IGBT desaturation may be higher compared to Case-1 and is coupled back through the reverse transfer capacitance, which is now higher at the low on-state voltage, and may result in a higher momentary rise of gate voltage. As a result the magnitude of the short circuit in Case-2 can reach significantly higher values than in Case-1.

In Figures 4.16, 4.17, 4.18, 4.19, and 4.20, the short circuit self limitation in Case-1 is shown as the dark area. Careful precautions must be considered in Case-2 to prevent the short circuit current magnitude going beyond a magnitude of ten times the rated current as an absolute limit (shaded area in Figures 4.16, 4.17, 4.18, 4.19, and 4.20).

Cautions:

1. *SCSOA is valid for gate pulse width, t_W, ≤ 10µs*
2. *SCSOA is a non-repetitive capability. Powerex IGBT modules can survive up to 100 short circuit events on a non-repetitive basis over the life of the equipment.*

Figure 4.15 Cases of Short-circuit

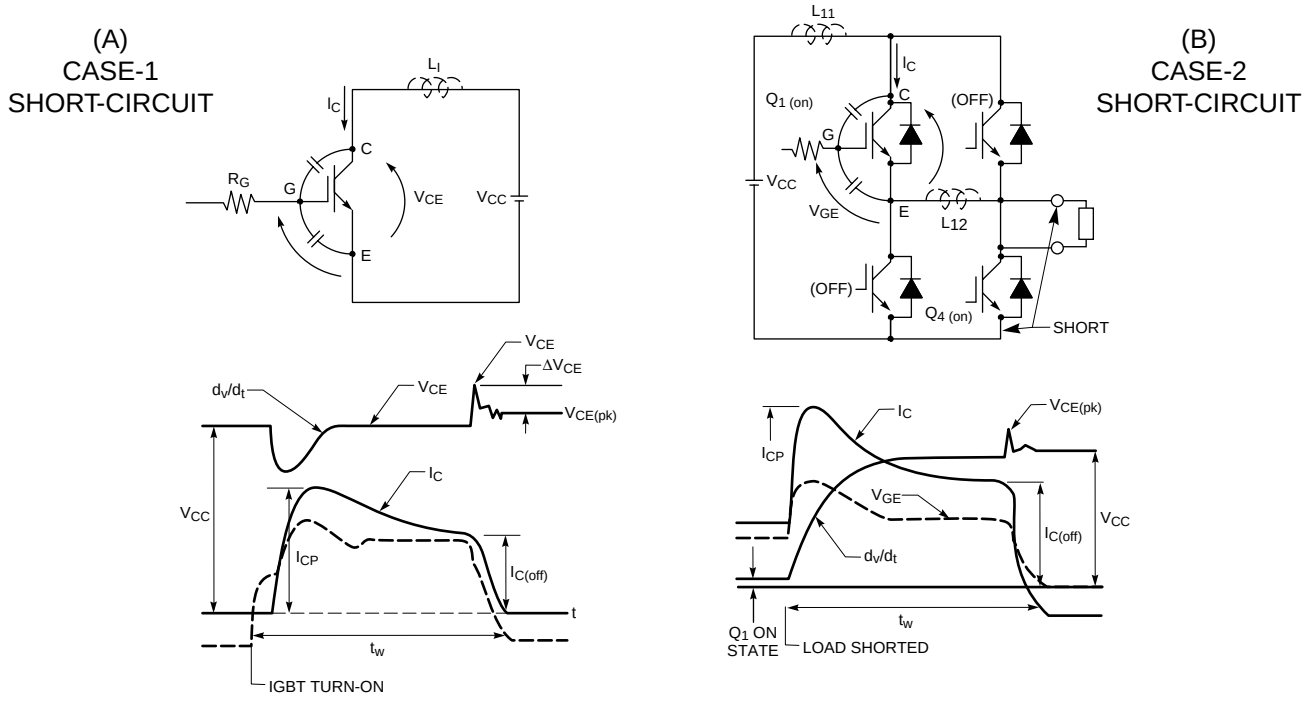


Figure 4.16 Short Circuit SOA for Modules 600V Class

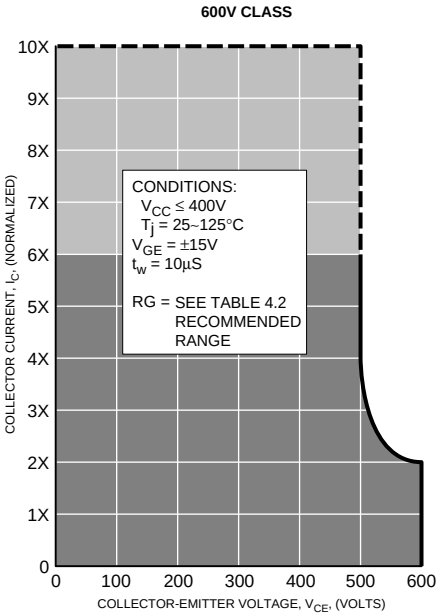


Figure 4.17 Short Circuit SOA for Modules 1200V Class

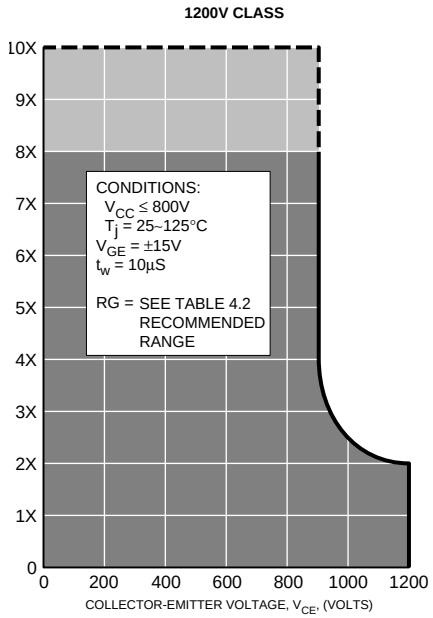


Figure 4.18 Short Circuit SOA for 1400V Modules

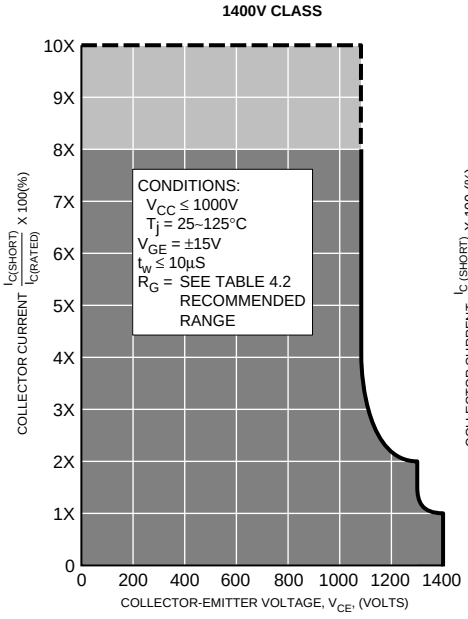


Figure 4.19 Short Circuit SOA for 1700V Modules

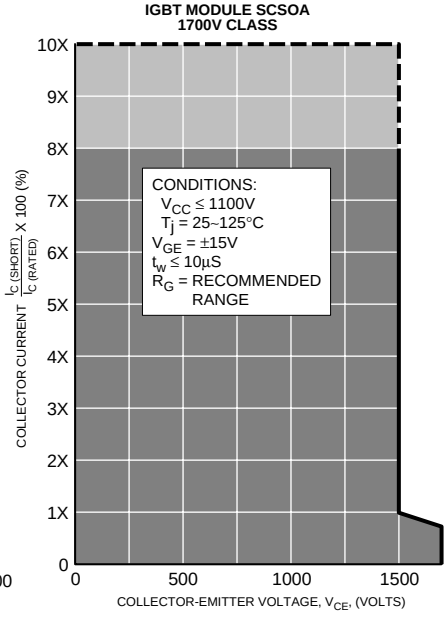
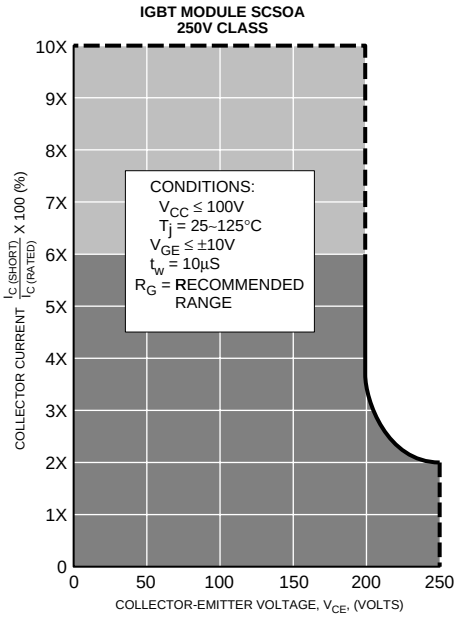


Figure 4.20 Short Circuit SOA for 250V Modules



4.3.3 RTC Circuit

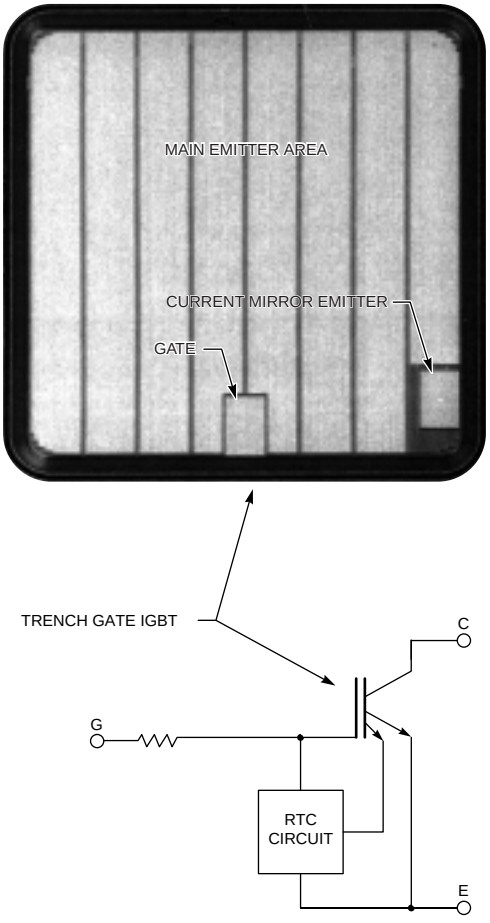
The F-Series trench gate IGBT chip by itself, has very limited short ciruit withstanding capability due to its extremely high short circuit saturation current. To reduce this current, the trench IGBT chip is fabricated with a current mirror emitter. The current mirror is connected to an RTC (Real Time Control) circuit to provide active clamping of short circuit current. The RTC and trench gate IGBT chip are shown in Figure 4.21. The RTC circuit is activated by the current from the current mirror emitter on the trench IGBT chip.

During a short circuit, the high current from the current mirror activates the RTC which reduces the gate driving voltage on the IGBT, thereby clamping the short circuit current to a safe level. The RTC circuit restores the short withstanding capability of the F-Series IGBT module.

4.4 Performance Curves

The characteristic curves show typical electrical characteristics and maximum transient thermal impedance characteristics of the IGBT and FWDi.

Figure 4.21 Trench Gate IGBT Chip and RTC



4.4.1 Output Characteristics

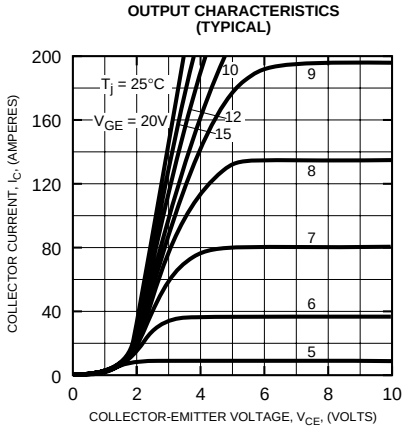
The output characteristics, as shown in Figure 4.22, define the value of V_{CE} that the IGBT will have when conducting a given I_C for a given value of V_{GE}. The IGBT is intended for switching operation only and the range for practical use is limited to the range of V_{CE} within the saturation area.

4.4.2 Collector-Emitter Saturation Voltage

V_{CE}(SAT) is a function of junction temperature, collector current, and gate-emitter voltage. Typically, the V_{CE}(SAT) of Powerex IGBTs decreases at low I_C with increasing temperature, that is, it has a negative temperature coefficient, whereas, after exceeding the crossover point the temperature coefficient becomes positive.

Figures 4.23 and 4.24 show typical collector-emitter saturation voltage characteristics, $V_{CE(sat)}$ versus I_C, and $V_{CE(sat)}$ versus V_{GE} respectively.

Figure 4.22



4.4.3 Device Capacitance

As the IGBT is a MOS gate device, it has three characteristic capacitances C_{ies}, C_{oes}, and C_{res}. These capacitances are specified in the data sheet because they are the most readily measured. They can be used to determine the IGBT junction and diffusion physical capacitance, C_{GE}, C_{GC}, and C_{CE}, by the formula given in Table 4.1 All three specified capacitances are small during device off state, but the large diffusion capacitance portion of the gate-collector capacitance causes them to increase dramatically during low collector-emitter states. (Figure 4.26) Input capacitance curves are drawn for V_{GE} = 0V.

Table 4.1

C_{ies} = C_{GE} + C_{GC} (in parallel) (measured C-E shorted)

C_{oes} = C_{CE} + C_{GC} (measured G-E shorted)

C_{res} = C_{GC}

4.4.4 Gate Charge

Since input capacitance varies with V_{CE} voltage, another parameter is used to better specify the energy required to turn on and off the IGBT, the gate charge, Q_G characteristic. The "Q_G vs. V_{GE}" curve shows the charge necessary to switch the IGBT. The first slope corresponds to the charging of the input capacitance while V_{CE} equals V_{CC}. When the V_{GE}(th) is achieved, the collector current, I_C, causes the V_{CE} to decrease towards V_{CE}(SAT). During the V_{CE} fall the C_{GC} capacitance increases rapidly and prevents the increase of V_{GE} as it draws more charge. When V_{CE} stabilizes, the input capacitance also stabilizes and the additional charge increases the V_{GE} voltage up to the full on level. At turn off the same charge quantity must be extracted.

4.4.5 Switching Characteristics

While the switching times given on the data sheets as electrical characteristics are for resistive load switching, the performance curves are for half-bridge inductive load. (See Figure 4.29) This reflects the fact that inductive loads are the most prevalent application for IGBTs. The switching times are defined in Figure 4.28B with $t_{on} = t_{d(on)} + t_r$ and $t_{off} = t_{d(off)} + t_f$. The turn-on delay time, $t_{d(on)}$, is the time required to attract excess electrons to the region just underneath the gate. The rise time, t_r, is the time required for collector current to increase from 10% of its final value to 90% of its final value. Rise time is basically

Figure 4.23

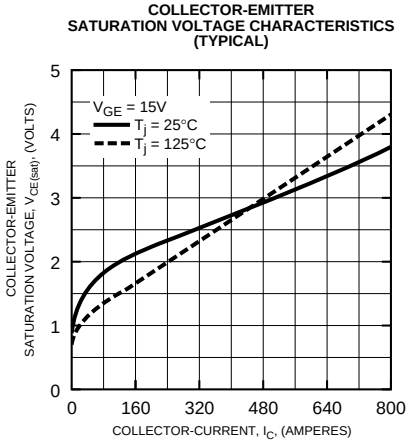


Figure 4.24

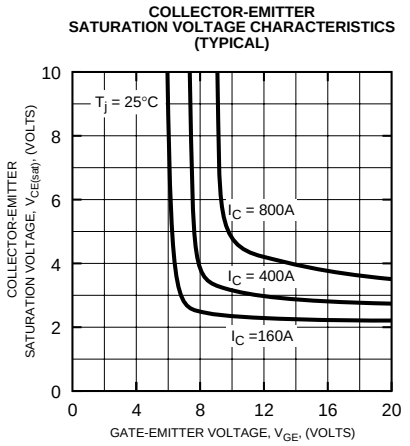


Figure 4.25 IGBT Device Capacitances

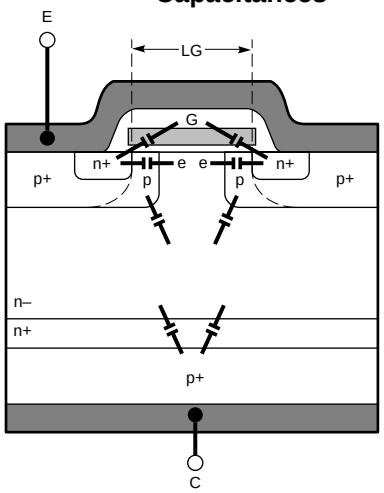


Figure 4.26 Typical IGBT Capacitances

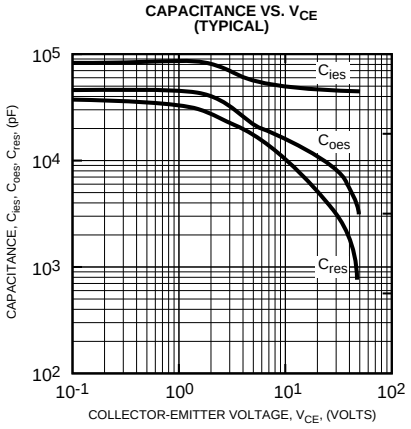
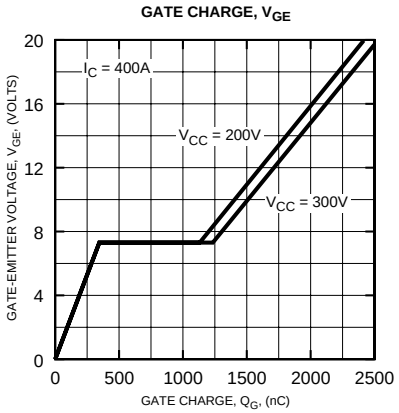


Figure 4.27 Typical Gate Charge



limited by gate impedance characteristics, which are partially a function of the gate contact geometry and partially a function of the input capacitances discussed previously. The turn-off delay time, $t_{d(off)}$ is due to gate capacitance limiting charges from leaving the under-gate area. Since charges are not required to leave the actual silicon crystal, as is the case with bipolar devices, turn-off delay time of an IGBT is considerably shorter than the storage time of bipolar devices. The fall time, t_f, is not limited by device capacitance. It includes the time necessary for recombination of excess charges stored in the n-bulk (tail period).

Figure 4.28 Measurement Circuit and Waveforms of Switching Time

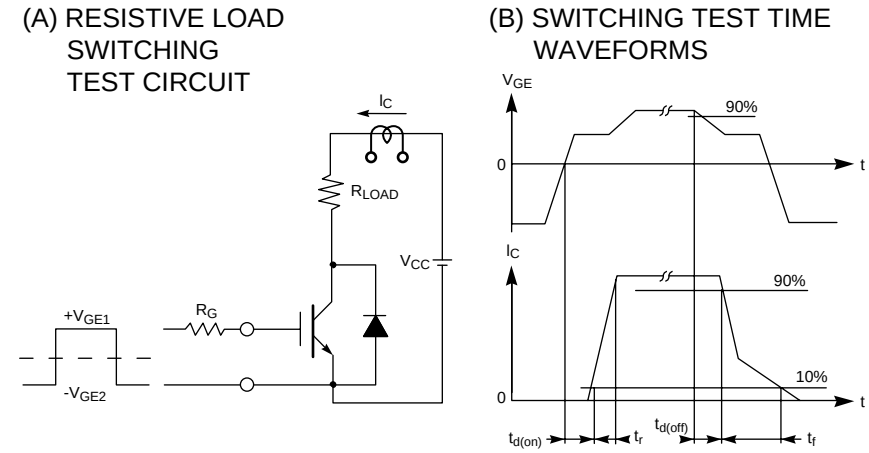
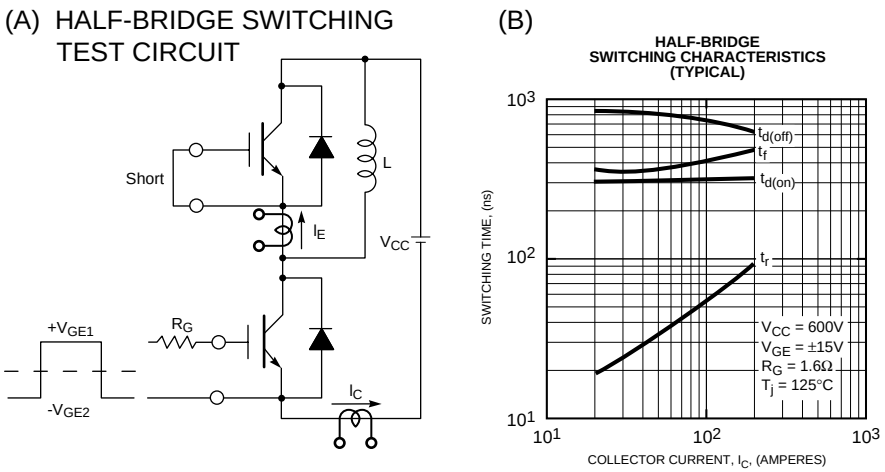


Figure 4.29 Half-bridge Switching Test (Inductive Load)



4.4.6 FWDi Characteristics

Characteristics of the diode part are shown in Figures 4.30 and 4.31. The diode part means the free-wheeling diode (FWDi) anti-parallel to the IGBT.

Figure 4.30 shows the voltage drop between anode and cathode when a forward current is supplied to the FWDi.

Typical reverse recovery characteristics of the FWDi are shown in Figure 4.31. These measurements are made using a circuit which operates as a half-bridge with inductive load as shown in Figure 4.29A. The low values of t_{rr} and I_{rr} and their relative independence of forward current are a unique feature of the FWDi used in Powerex IGBT modules.

4.4.7 Transient Thermal Impedance

The transient thermal impedance, $Z_{th(j-c)}$ gives the rise of junction temperature over case temperature per unit of power applied for a given time period as shown in Figures 4.32 and 4.33. The value of $Z_{th(j-c)}$ is obtained by multiplying the value of $R_{th(j-c)}$ by the normalized factor taken from the curve at the time of interest. The steady state thermal resistance, $R_{th(j-c)}$ is the saturated value of $Z_{th(j-c)}$. If this value is smaller, the maximum allowable power loss, P_C, of a device becomes larger:

$$P_C = \frac{T_j(max) - T_C}{R_{th(j-c)}}$$

4.4.8 Switching Energy Characteristics

Switching energy curves are provided in order to simplify estimation of switching losses. Use of these curves is described in more detail in Section 3.4.1 of this application data. Figures 4.34 through 4.44 show turn-on and turn-off switching energy as a function of collector current for Powerex 250V, 600V, 1200V, 1700V H-Series and U-Series and F-Series IGBT modules. Figures 4.45 and 4.48 show switching loss versus series gate resistance for U-Series and F-Series IGBT modules.

4.5 IGBT Selection

Proper selection of an IGBT involves two key points. Both are related to keeping the IGBT within its maximum ratings during operation. The first criterion is that the peak collector current during operation including any required overload current must be within the SWSOA (this means < 2 x I_{rated} or 2 x nameplate current). The suggested IGBT selections in Sections 2.3, 2.4, and 2.5 are based on a 200% overload requirement and allow 20% for ripple current factors in determining the peak IGBT current requirement for the inverter. The second criterion is that the IGBT operating junction temperature must always be kept below $T_{j(max)}$ (150°C) in all normal operation including expected motor overload. Power dissipation and thermal design considerations are discussed in detail in Section 3.4. Modules selected for listing in Sections 2.3, 2.4, and 2.5 will meet these requirements with normal environmental and heatsink considerations. It may be possible (or required) to use a lower (higher) current rated if more (or less) efficient cooling is employed.

4.6 IGBT Module Gate Drive

IGBTs require gate voltage to establish collector to emitter conduction. This gate voltage can be applied by a variety of drive circuits. The parameters to be considered in selecting a drive circuit include device off biasing requirements, gate charge requirements, ruggedness requirements and power supply availability.

A recommended drive circuit includes substantial on biasing and off biasing. Such a circuit is shown in Figure 4.49. The IGBT gate-emitter impedance is large enough that turn-on can be accomplished with MOSFET drive techniques, but as the IGBT input capacitance is larger than for a MOSFET the IGBT turn-off bias should be stronger than many MOSFET drives offer.

Figure 4.30

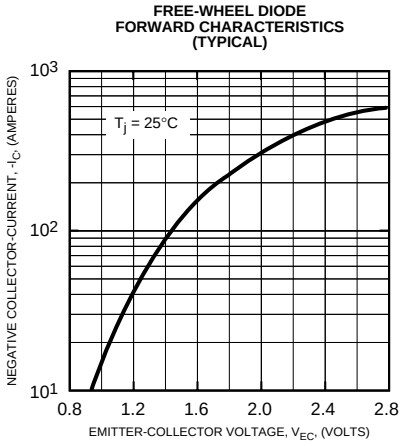


Figure 4.31

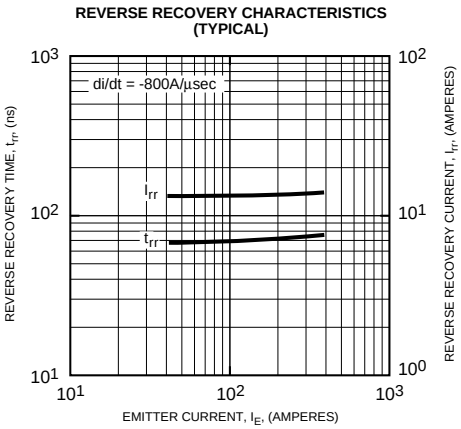


Figure 4.32

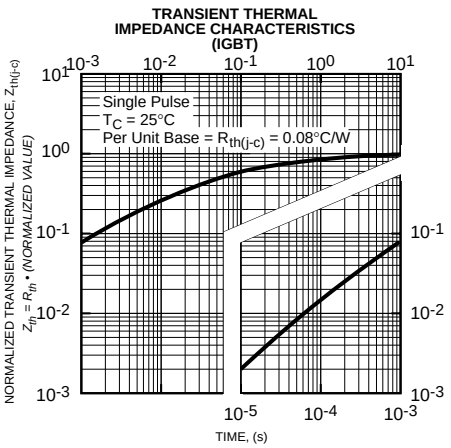


Figure 4.33

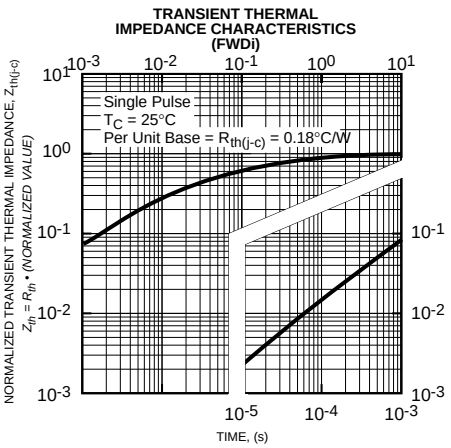


Figure 4.34

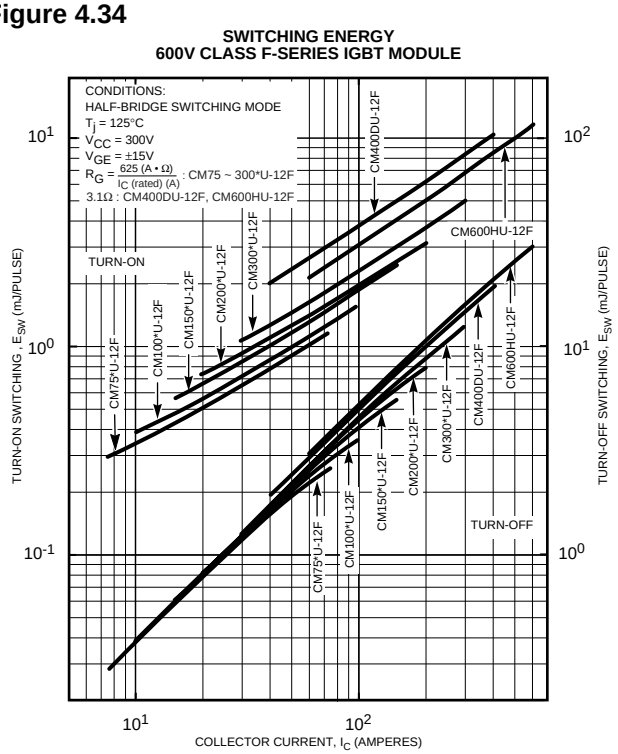


Figure 4.35

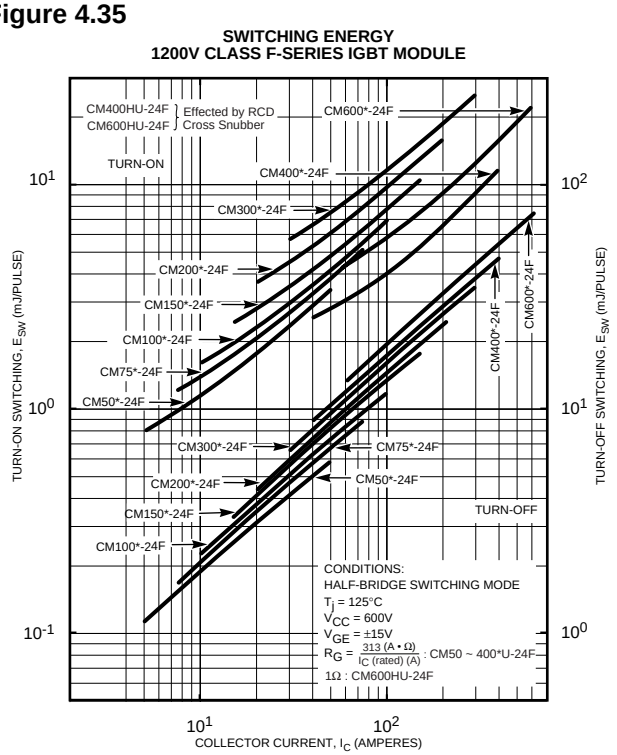


Figure 4.36

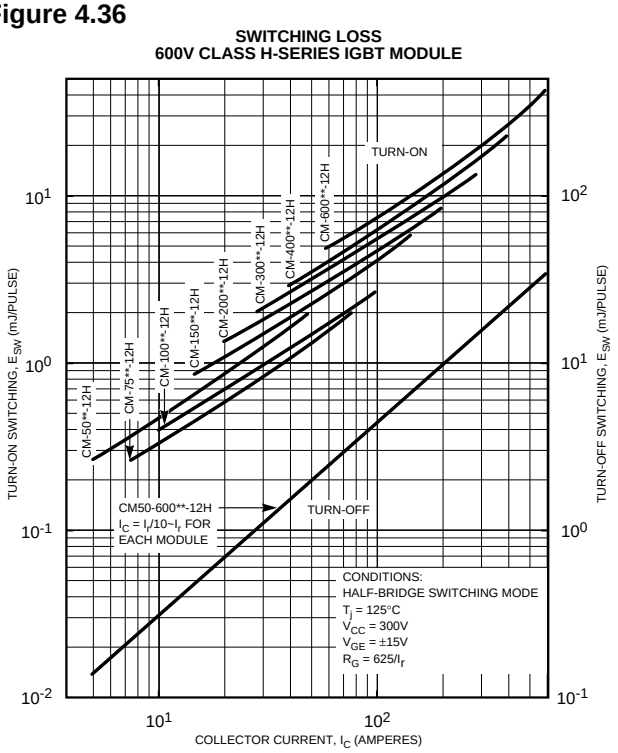


Figure 4.37

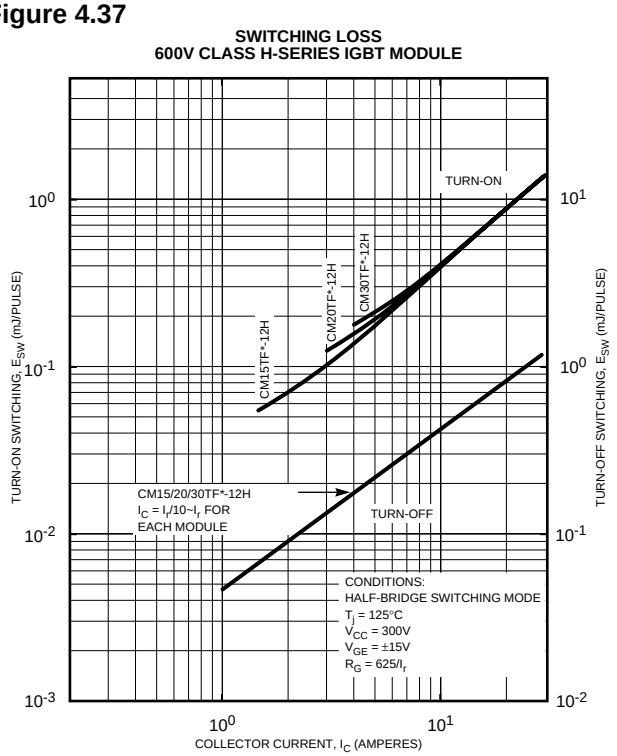


Figure 4.38

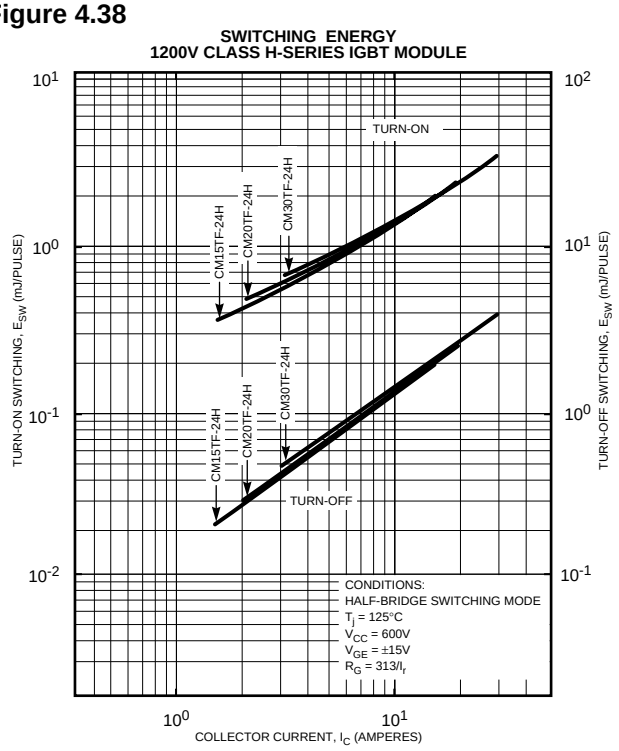


Figure 4.39

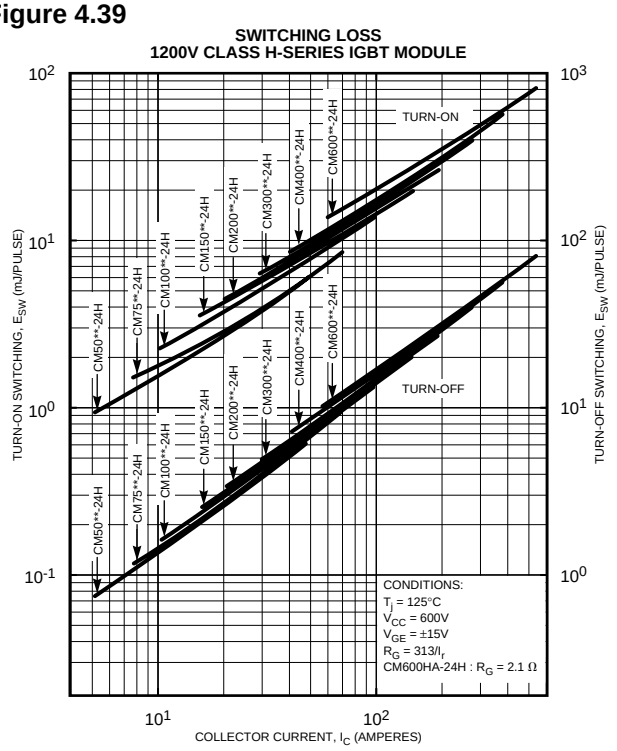


Figure 4.40

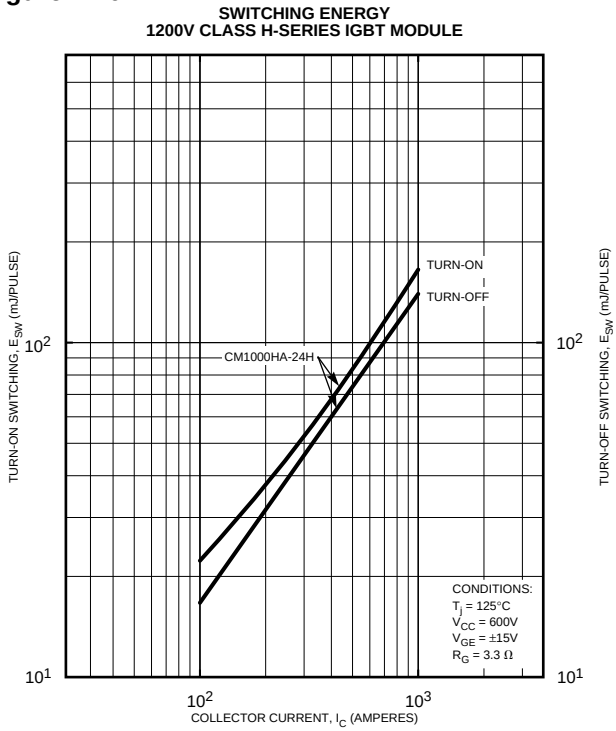


Figure 4.41

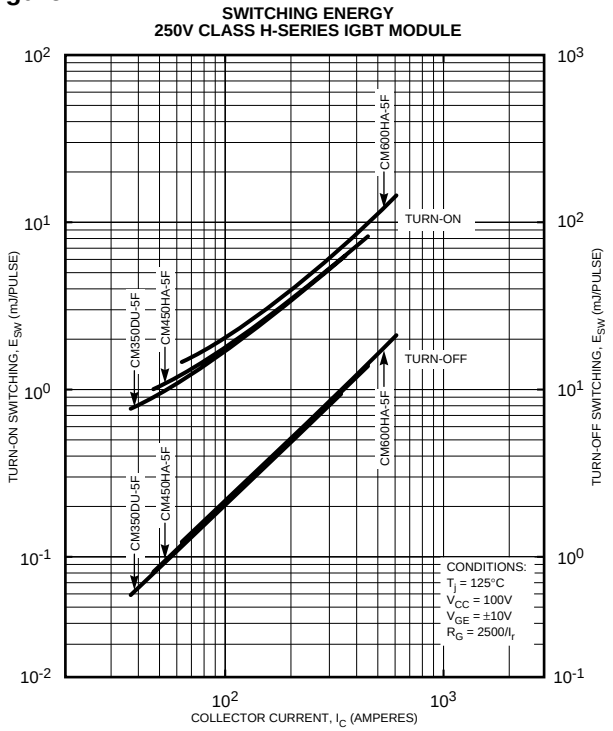


Figure 4.42

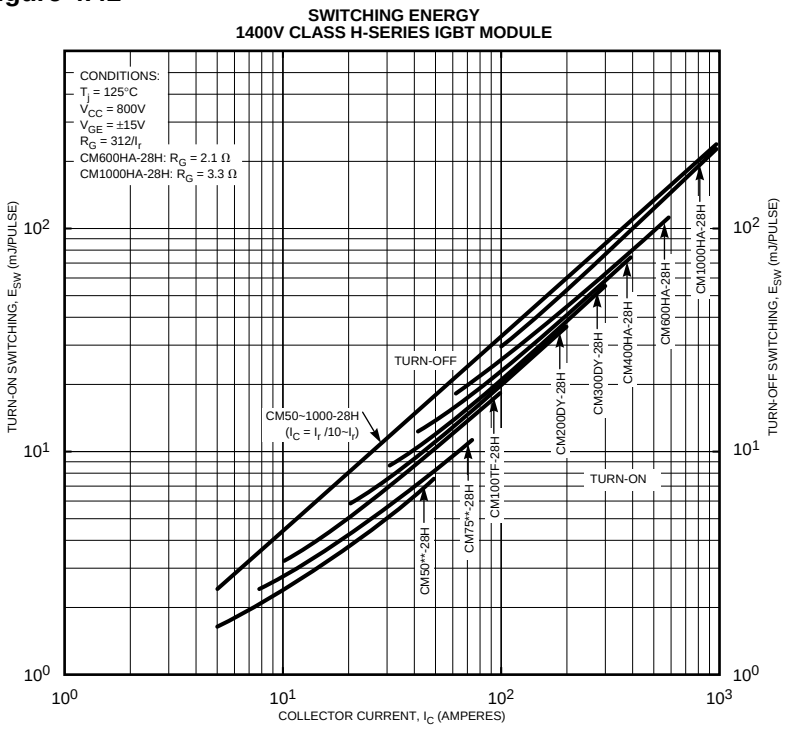


Figure 4.43

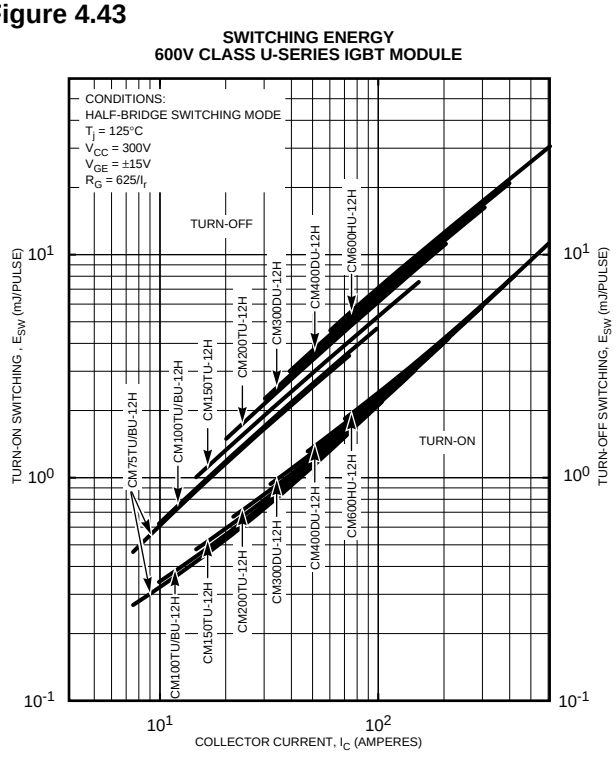


Figure 4.44

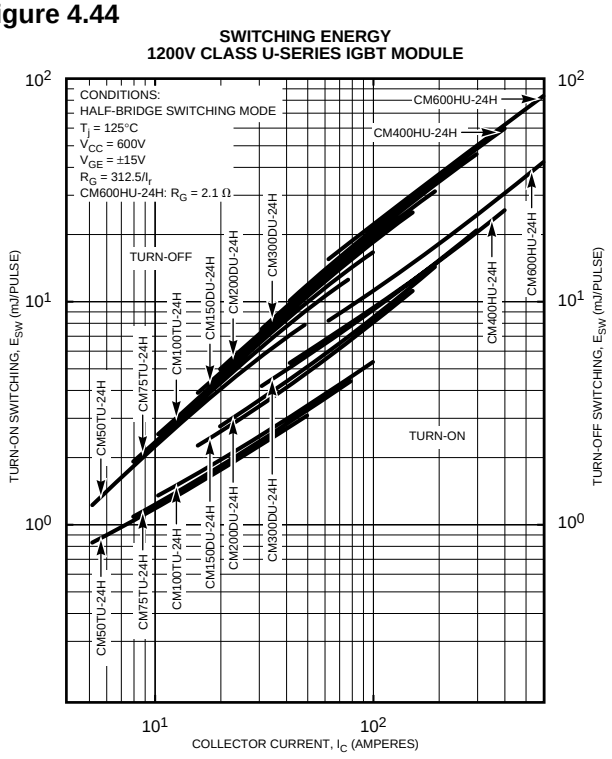


Figure 4.45

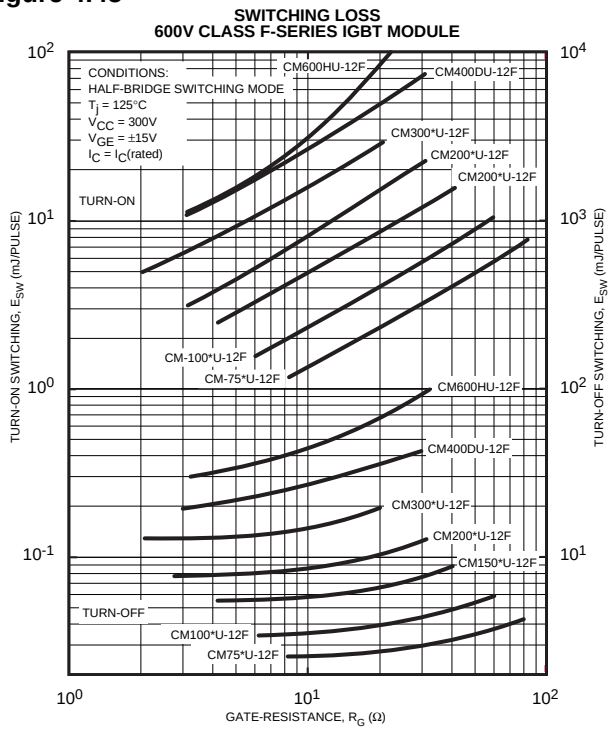


Figure 4.46

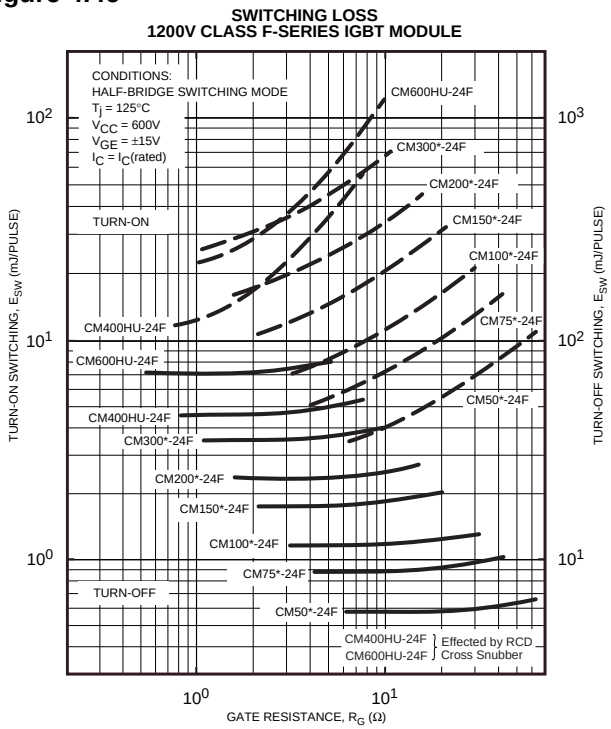


Figure 4.47

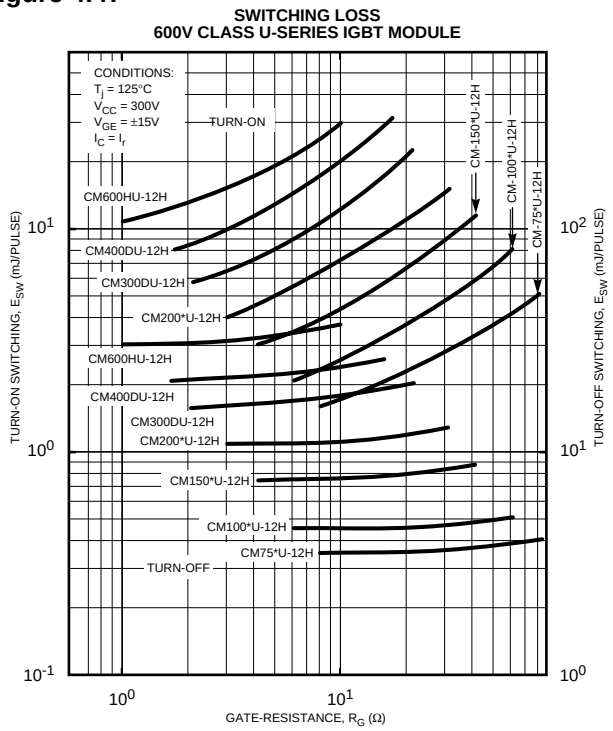
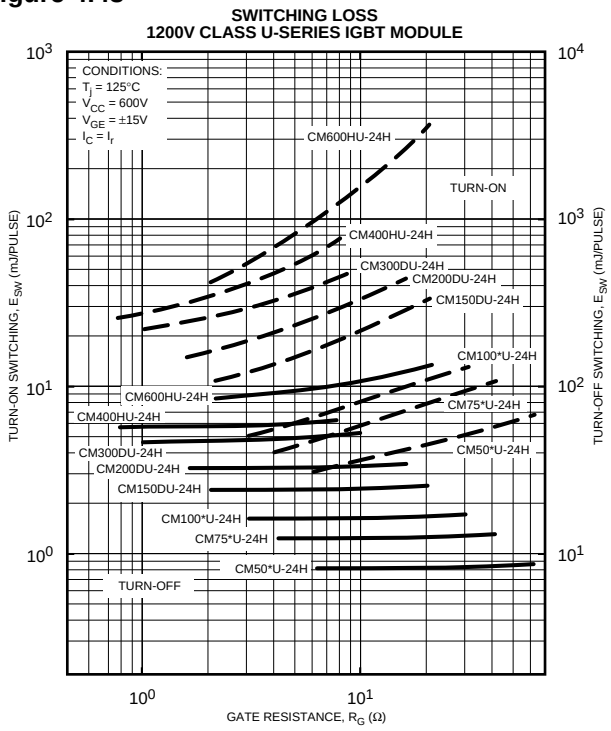


Figure 4.48



4.6.1 Gate Drive Voltage

For turn-on a positive gate voltage of 15V ±10% is recommended. This value is sufficiently high to fully saturate the IGBT at rated current and minimize on-state losses while it is sufficiently low to limit short circuit current and its resulting power stress. In no case should a gate drive outside of the range of 12 to 20V be used for turn-on.

An IGBT will be off when its gate voltage is zero. However, in order to ensure that the IGBT stays in its off state when dv/dt noise is present in the collector-emitter voltage an off bias must be used. Use of reverse bias also decreases turn off losses. The relationship between reverse bias voltage and switching losses is shown in Figure 4.50. For Powerex IGBTs an off bias of -5 to -15V is recommended.

Powerex IGBT modules are not suitable for linear operation. Gate voltages in the 3 to 11V range should only appear on the IGBT's gate during rapid switching transitions.

4.6.2 R_g - Series Gate Resistance

Selecting the proper series gate resistor for IGBT gate drive is very important. The value of the gate resistor has a significant impact on the dynamic performance of the IGBT. The IGBT is turned on and off by charging and discharging the gate capacitance. A smaller gate resistor will charge/discharge the gate capacitance faster, reducing the switching times and switching losses. Figures 4.51 and 4.52 depict the typical dependence of switching times and losses on the value of the series gate resistor.

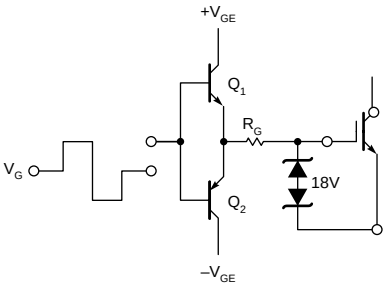
Under short circuit or during turn off of the free-wheeling diode across an IGBT, the dv/dt applied to the IGBT and its collector to gate capacitance can cause a current to flow in the gate circuit. If this current is large enough the voltage developed across the gate resistor can cause the IGBT to turn on. So, while smaller gate resistances offer enhanced ruggedness (rejection of dv/dt turn on), they also provide less margin for noise and can lead to oscillation problems in conjunction with the gate-emitter capacitance and any parasitic inductance in the gate drive wiring.

In addition, smaller gate resistors allow faster turn-on di/dt of the IGBT. This may cause high dv/dt and increased surge voltage at FWDi recovery.

Giving consideration to all of the above effects, Table 4.2 gives the recommended values of series gate resistance. The value given for the minimum series gate resistor is the standard resistor that is used for determining all data sheet parameters and characteristics. The maximum value given allows for flexibility in slowing down the switching speed and avoiding potential oscillation problems without risking linear operation. It also provides for slower switching in lower frequency applications where switching losses are not as critical and reduced transient voltages and gate drive current requirements may be a factor.

Table 4.2 was generated considering hard switched inductive load applications which

Figure 4.49 Typical IGBT Gate Drive Circuit



Q_1, Q_2: $V_{CEO} \geq 50V$

$$I_{C,\,Max.} \geq \frac{|V_{GE}^{+}| + |V_{GE}^{-}|}{R_G}$$

R_G: See Table 4.2 or data sheet for suggested value

Figure 4.50 Switching Energy as a Function of Reverse-Bias Voltage

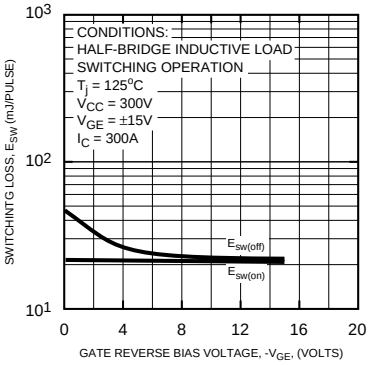


Figure 4.51 Typical Dependence of Switching Time on Gate Resistance

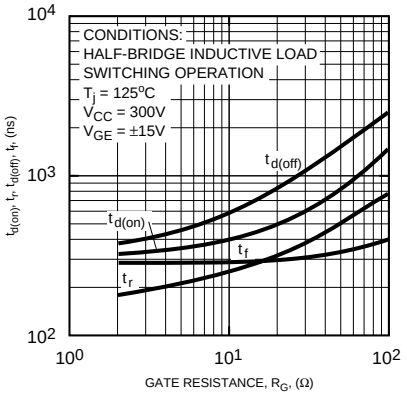
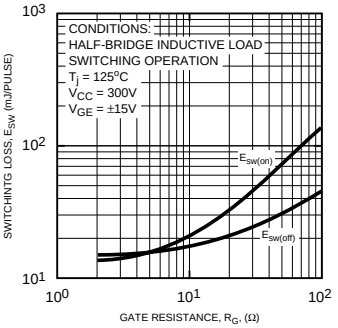


Figure 4.52 Typical Dependence of Switching Loss on Gate Resistance



represent the majority of IGBT applications. There are some low frequency, chopper, and resonant mode applications for which values of series gate resistance outside of the limits in the table may be used. Consult the factory for specific recommendations in these cases.

4.6.3 Gate Drive Power Requirements

IGBT switching consumes power from the gate drive power supply as a function of the transition from negative to positive bias, Δ_{GE}, the total gate charge, Q_G, and the frequency of operation, f. The minimum peak current capability, $I_G(pk)$ of the supply is:

$$I_G(pk) = \pm \frac{\Delta V_{GE}}{R_g}$$

The average power, P_{AVG}, required of the supply is:

$$P_{AVG} = \Delta V_{GE} * Q_G * f$$

where

ΔV_{GE} = $V_{GE(on)} + |V_{GE(off)}|$
Q_G = Total Gate Charge (See Figure 4.53)
f = Switching Frequency

Table 4.2 Values of Gate Resistance

Recommended Series Gate Resistance, R_G, (ohms)			
Voltage (Volts)	Type Number	Turn-on Min.	Turn-on Max
600	CM15**-12H	42	420
	CM20**-12H	31	310
	CM30**-12H	21	210
	CM50**-12H	13	130
	CM75**-12H & F	8.3	83
	CM100**-12H & F	6.3	63
	CM150**-12H & F	4.2	42
	CM200**-12H & F	3.1	31
	CM300**-12H & F	2.1	21
	CM400**-12H	1.6	16
	CM400DU-12F	3.1	31
	CM600**-12H	1.0	10
	CM600HU-12F	3.1	31
1200	CM15**-24H	21	210
	CM20**-24H	16	160
	CM30**-24H	10	100
	CM50**-24H & F	6.3	63
	CM75**-24H & F	4.2	42
	CM100**-24H & F	3.1	31
	CM150**-24H & F	2.1	21
	CM200**-24H & F	1.6	16
	CM300**-24H & F	1.0	10
	CM400**-24H	0.78	8
	CM-400HU-24F	0.78	7.8
	CM600**-24H	2.1	22
	CM600HU-24F	1.0	10
	CM1000**-24H	3.3	33
1400	CM50**-28H	6.3	63
	CM75**-28H	4.2	42
	CM100**-28H	3.1	31
	CM200DY-28H	1.6	16
	CM300DY-28H	1.0	10
	CM400HA-28H	0.78	8
	CM600HA-28H	2.1	22
	CM1000HA-28H	3.3	33
1700	CM400HA-34H	10	50

4.6.4 Gate Drive Layout Considerations

Gate drive layout is critical to avoid potential oscillations, slow rise of gate voltage, loss of noise immunity, sag in gate supply voltage, or reduction in efficiency of the gate protection circuitry.

Guidelines that should be followed in designing the gate drive layout are:

1. The layout must minimize the parasitic inductance between the driver's output stage and the IGBT. This corresponds to keeping the loop area as small as possible in the indicated section of Figure 4.54.

2. Care must be taken to avoid coupling of noise between the power circuit and the control circuit. This can be accomplished by proper placement of the gate drive board and/or shielding the gate drive circuit.

3. It is recommended to use the auxiliary emitter terminal for connecting the gate drive.

4. If direct connection of the drive PCB to the IGBT control terminals is not possible, the use of twisted pair (3 turns per inch of minimum length) or stripline is recommended.

5. Gate protection clamp (described in Section 4.7.1) must also have low inductance layout and must be located as close as possible to the gate-emitter control terminals of the IGBT module.

6. Do not route printed circuit board traces near each other that are subjected to mutual potential changes due to IGBT switching. High dv/dt can couple noise through parasitic capacitances. If crossing or parallel routing of those traces is unavoidable, use shield layers in between.

7. Parasitic capacitance between high side gate drive circuits, high and low side gate drive circuits and control circuits may cause problems with coupled noise. Power supply transformer inter-winding capacitance can be another source of coupled noise. Appropriate measures to reduce these parasitic capacitances have to be implemented.

8. If optocouplers are used for isolation of the high side gate drive signals they should have a minimum common mode transient immunity of 10,000 V/μs.

4.7 Protecting IGBT Modules

4.7.1 dv/dt Protection

In half-bridge and inductive mode operation the IGBT that is in the off state is subjected to sharp rise of positive voltage due to recovery of its anti-parallel diode as shown in Figures 4.55 and 4.56. This static dv/dt can be higher than the rate of rise of V_{CE} at turn off of the IGBT. This dv/dt generates a current in the collector gate capacitance that flows into the gate drive circuit as shown in Figure 4.57. Although the gate is reverse biased in the off-state, this current causes an increase of V_{GE} towards $V_{GE(th)}$ due to the gate circuit impedance. In the worst case, the threshold voltage is reached at the IGBT chip and turn on of the IGBT is initiated resulting in an arm shoot through. The requirements to avoid this untimely turn on are:

1. $V_{G(off)}$ should be sufficiently negative. (See Table 4.3)

2. R_g in off-state should be low. (Recommended values are given in Table 4.2.)

3. Gate circuit inductance, L_G, should be minimized.

Figure 4.53 Total Gate Charge in IGBT Switching

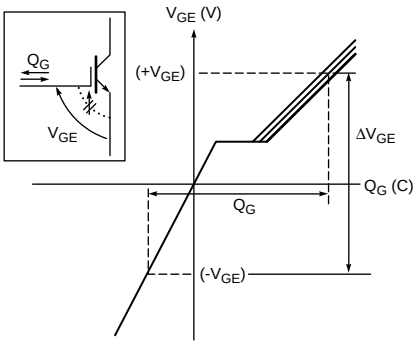


Figure 4.54 Gate Drive Layout

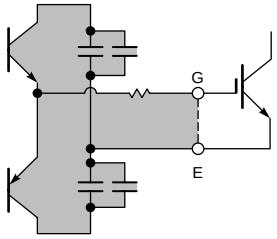


Table 4.3 Recommended Gate Off-bias

V_{CES} Rating	Minimum $V_{GE(off)}$	Recommended $V_{GE(off)}$
600V	-2V	-5 to -15V
1200V	-2V	-5 to -15V
1400V	-5V	-5 to -15V
1700V	-5V	-5 to -15V

4.7.2 Short Circuit Protection

If a short circuit occurs the stress on the IGBT must remain within the SCSOA as shown in Section 4.3.2. Common methods of short circuit protection are current sensing as shown in Figure 4.58 and desaturation detection as shown in Figure 4.59.

Once a short circuit is detected, several techniques can be employed to protect the IGBT from destruction. The most elementary technique is to simply turn off the IGBT within 10ms. But, in this case, the snubber or clamp must be designed for the short circuit condition. However, it is recommended to use turn-off techniques that control the V_{GE} in order to reduce the stress on the IGBT. These techniques are:

1. **Controlled Shutdown:**
   The gate voltage is reduced either in steps or by a ramp so the short circuit current is reduced and its di/dt is also reduced as the IGBT turns off. The spike voltage is also reduced.

2. **V_{GE} Clamping:**
   As described in Section 4.3.2 the peak of the short circuit current depends on V_{GE} which is augmented by the feedback of dv/dt through the gate-collector capacitance. The effect can be overcome by

Figure 4.55 One-phase Circuit of an Inverter Bridge (Inductive Load)

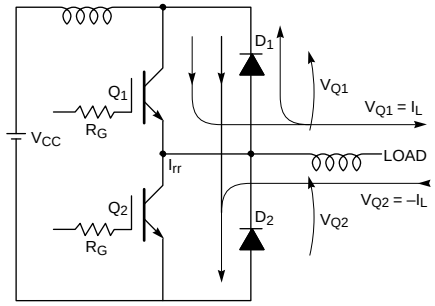


Figure 4.56 Relevant Current and Voltage Waveforms of Phase Elements

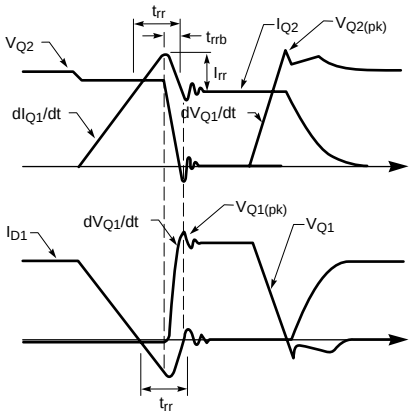
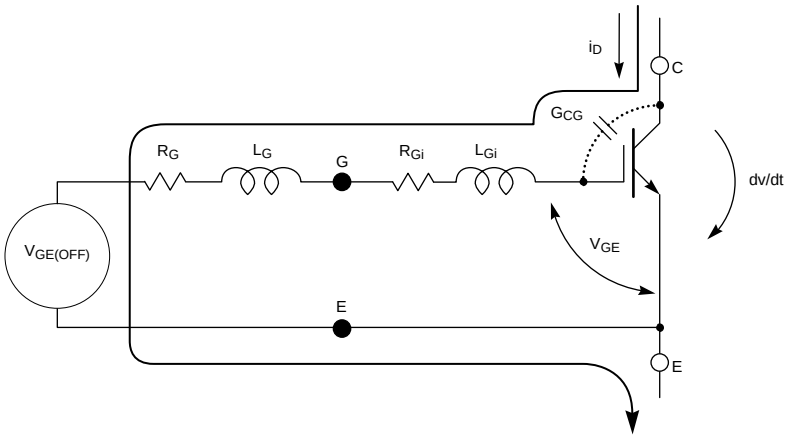


Figure 4.57 dV/dt Effect on IGBT Gate Circuit



clamping the V_{GE} safely below 18 Volts. An effective clamping circuit is shown in Figure 4.60. The clamping diode, D_{CL}, and clamping capacitor, C_{CL}, should be connected directly to the control signal terminals of the IGBT module. A fast forward recovery is required for D_{CL}. For low current IGBTs a zener clamp between gate and emitter may also be effective.

3. Reducing t_W:
For reducing the thermal stress in short circuit operation it is beneficial to reduce the time in short circuit, t_W. However, this will increase the magnitude of the current at turn off as shown in Figure 4.61, and di/dt will be increased. This undesirable effect may be overcome by using the techniques in Steps 1 and 2 above.

Caution:
The above techniques reduce the stress at short circuit turn-off. However, they do not release the designer from considering worst case turn off in snubber design.

4.7.3 Handling Precautions

Since IGBT gates are insulated from any other conducting region, care should be taken to prevent static build up which could possible damage gate oxides. All ESD sensitive IGBT modules are shipped from the factory with conductive foam contacting the gate and emitter control terminals. Never touch the gate terminals during assembly and keep the conducting foam in place until permanent connections are made to the gate and emitter control terminals. Always ground parts

Figure 4.58 Short Circuit Protection Scheme (Example)

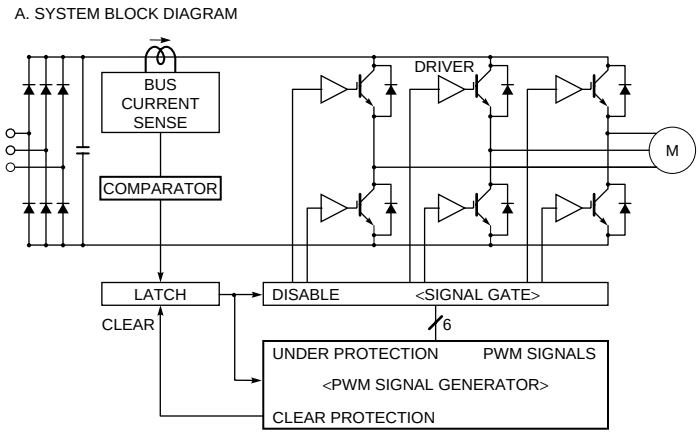
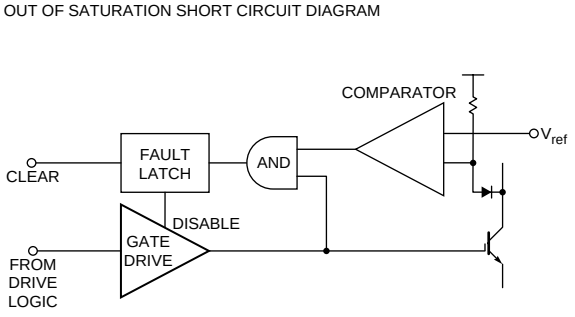


Figure 4.59 Out of Saturation Short Circuit Protection



touching gate terminals during installation. In general, standard ESD precautions applicable to MOSFETs should be followed.

Other handling precautions that should be observed are:

1. Use grounded work station with grounded floors and grounded wrist straps when handling devices.

2. Use a 100Ω resistor in series with the gate when performing curve tracer tests.

3. Never install devices into systems with power connected to the system.

4. Use soldering irons with grounded tips when soldering to gate terminals.

4.8 Parallel Operation

Powerex IGBT modules can be connected in parallel for applications requiring very high currents. In such applications parallel operation should only be considered when the highest current module available is not large enough. Use of a single large module rather than smaller parallel modules is recommended because it eliminates concerns about static and dynamic current balance among the paralleled devices. With proper attention to circuit design and device selection several modules can be reliably operated in parallel. The following sub-sections outline the basic requirements and considerations for parallel operation of single IGBT modules with ratings of 200A or more.

Figure 4.60 V_{GE} Clamping Circuit

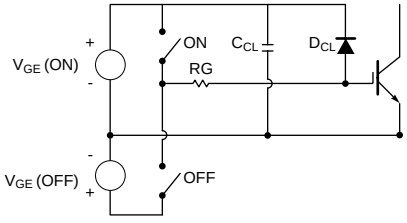
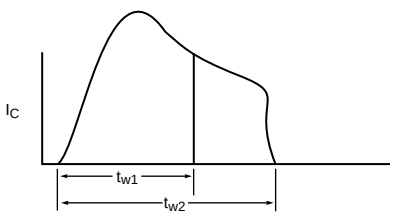


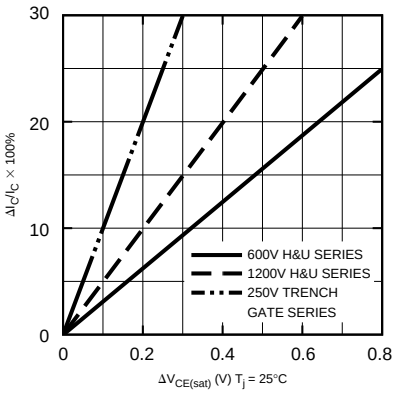
Figure 4.61 Short Circuit at Reduced t_W



4.8.1 Static Current Balance

Table 4.4 outlines the factors influencing parallel operation of IGBT modules. Under static on-state or DC operating conditions the collector to emitter saturation voltage and junction temperature have the biggest influence on current sharing. To achieve reliable and consistent static current balance devices should be mounted on the heat sink near to each other with cooling arranged to maintain uniform base plate temperatures between paralleled modules. A good general design guideline is to maintain a base plate temperature difference between paralleled devices of 15°C or less. Parallel connected devices should be selected with matched saturation voltages. The maximum static current imbalance as a function of saturation voltage at T_j = 25°C is shown in Figure 4.62. Experimental analysis has demonstrated that the current balance becomes considerably better at elevated junction temperatures. For example, in the case of 1200V H-series the worst case imbalance drops from 15% at 25°C to about 5% at 125°C. Figure 4.63 shows how the imbalance shown in Figure 4.62 is defined. To facilitate the matching of devices for parallel operation Powerex provides IGBT modules marked with a saturation voltage rank letter. All devices to be operated in parallel should have the same saturation voltage rank. Devices can also be supplied in matched sets for parallel applications. Contact the factory for ordering information. Table 4.5 shows the standard saturation voltage letter rankings for Powerex IGBT modules. Column 1 of this table is applicable to all voltage classes of U-Series and H-Series modules, column 2 applies to 250V trench gate IGBT modules, and column 3 applies to 600V and 1200V F-Series modules. Note that all ranks do not exist for a given voltage class. For example, 600V H-Series modules have a maximum data sheet saturation voltage of 2.8V and therefore ranks

Figure 4.62 Maximum Current Imbalance vs. DV_{CE}(sat)



H through M do not exist for these devices. Saturation voltage ranks are intended for matching sets of devices for parallel applications. Orders specifying a specific rank will not normally be accepted. The saturation voltage rank will be either marked with white ink on the top of the module or indicated on the label. Saturation voltage ranking is available for single modules rated 200A or more.

Saturation voltage ranking is not normally available for dual or six pack types. Modules of different saturation voltage ranks may be used in the same inverter provided that devices connected in parallel are of the same rank.

When modules of the same saturation voltage rank are paralleled the static current imbalance will be minimized so that the following recommended deratings can be applied:

For 250V Trench Gate derate I_C by 10%
For 600V Class H-Series, U-Series and F-Series derate I_C by 10%
For 1200V and 1400V Class H-Series, U-Series and F-Series derate I_C by 15%
For 1700V Class H-Series derate I_C by 20%

Table 4.4 IGBT Module Parallel Operation, Current Sharing

Factors related to current sharing and their effect.

		Categories of Current Sharing			
		IGBT Switching		Steady State	
Factors Effecting Current Sharing		Turn-on	Turn-off	di/dt = 0	di/dt ≠ 0
Device Characterization	ΔV_{CE}(SAT)	X	X	●	X
	Δ Temperature	●	●	●	X
Main Circuit	ΔL (Supply to Device)	●	∂	X	X
Wiring Inductance	ΔL (Total Loop Including Load)	X	X	X	●
Driver Wiring	Driver to Device Wiring Length Diff.	●	●	X	X
	Output Impedance of Driver	●	●	X	X

● - Relation Exists **X** - No Relation ∂ - Relation Ambiguous or Weak

Figure 4.63 Circuit Showing the Definition of Current Imbalance

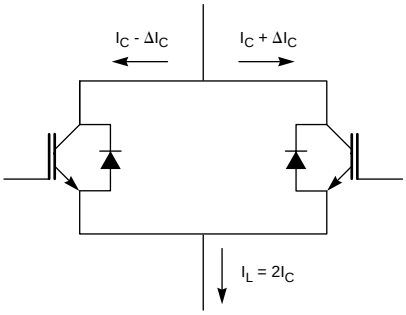


Table 4.5 Saturation Voltage Ranks for Parallel Applications

Saturation Voltage Ranks for H-Series and U-Series IGBT Modules		Saturation Voltage Ranks for 250V Trench Gate IGBT Modules		Saturation Voltage Ranks for 600V and 1200V F-Series Modules (CM**-12F / CM**-24F)	
Saturation Voltage Rank	$V_{CE(sat)}$ (V) I_C = Rated Current V_{GE} = 15V T_j = 25°C	Saturation Voltage Rank	$V_{CE(sat)}$ (V) I_C = Rated Current V_{GE} = 15V T_j = 25°C	Saturation Voltage Rank	$V_{CE(sat)}$ (V) I_C = Rated Current V_{GE} = 15V T_j = 25°C
C	1.70 ~ 1.95	Q	1.15 ~ 1.30	E	1.5 ~ 1.6
D	1.90 ~ 2.15	R	1.25 ~ 1.40	F	1.55 ~ 1.65
E	2.10 ~ 2.35	S	1.35 ~ 1.50	G	1.6 ~ 1.7
F	2.30 ~ 2.55			H	1.65 ~ 1.75
G	2.50 ~ 2.80			J	1.7 ~ 1.8
H	2.75 ~ 3.05			K	1.75 ~ 1.85
J	3.00 ~ 3.30			L	1.8 ~ 1.95
K	3.25 ~ 3.55			M	1.9 ~ 2.05
L	3.50 ~ 3.80			N	2.0 ~ 2.2
M	3.75 ~ 4.05			P	2.15 ~ 2.4

When more than two modules are paralleled the derating can be computed using the following formula:

$$\% \text{ Derating} = \left[1 - \frac{\left(\frac{(n-1)(1-x)}{(1+x)}\right) + 1}{n}\right] \times 100$$

Where:

x = 0.1 for 250V devices
x = 0.1 for 600V devices
x = 0.15 for 1200V/ 1400V devices
x = 0.20 for 1700V devices
n = number parallel

Example:

In the case of four IGBT modules of 600V class connected in parallel, the formula is:

$$\% \text{ Derating} = \left[1 - \frac{\left(\frac{(4-1)(1-.1)}{(1+.1)}\right) + 1}{4}\right] = 13.6\%$$

So the derated current with 4 parallel 300A modules is:

300A(1 - 0.136) x 4 = 1037A

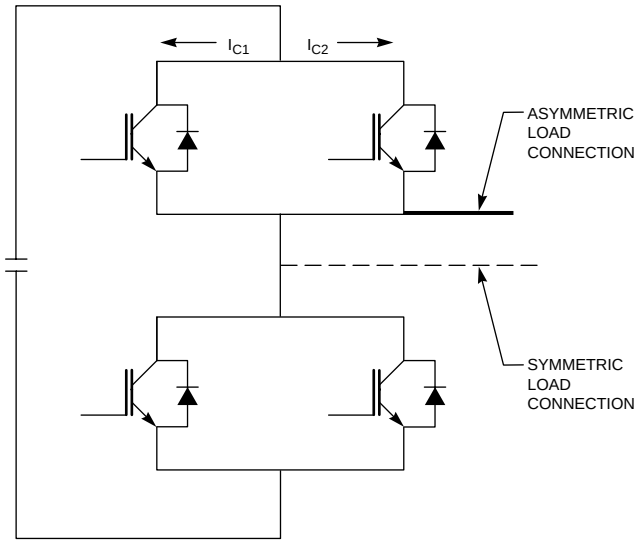
4.8.2 Dynamic Current Balance

Matching $V_{CE(sat)}$ is effective for maintaining good static steady state current balance. This matching also helps some with turn off current balance because of the fundamental inverse relationship of fall time and saturation voltage. However, as indicated in Table 4.4, gate drive conditions and power circuit layout have by far the greatest impact on dynamic current balance between paralleled devices. Temperature differences between paralleled modules is also a factor because of the resulting effect on delay time and therefore the design guidelines given in Section 4.8.1 should be observed for dynamic current balance as well. To understand the circuit layout factors affecting dynamic current balance it is necessary to consider two cases:

The first case is when the device is in the static on-state and the load current is changing. As indicated in Table 4.4 the main cause of imbalance in this case is differences in inductance to the load connection. In practical applications this is most often the result of an asymmetric connection of the load as shown in Figure 4.64. A typical current imbalance waveform resulting from an asymmetric load connection is shown in Figure 4.65. Experimental analysis has shown that this type of imbalance can also be caused by the orientation of the main circuit bus bars. For example, if the load connection causes the load current to run in parallel with the current in one of the paralleled modules mutual inductance effects can cause the inductance of that path to be effectively reduced or increased even though the mechanical connection point is symmetric.

The second case that must be considered is current imbalance that occurs at the moment of turn-on or turn-off switching. Table 4.4 indicates that the most important factors influencing current balance are the gate circuit design and module temperature. The recommended gate drive configuration for paralleled modules is shown in Figure 4.66. The recommended approach is to use a single drive stage with a separate R_g for each paralleled module. The small kelvin emitter connections on the paralleled devices should be connected with a short, low impedance symmetric connection in order to prevent ground loop currents from

Figure 4.64 Circuit Diagram Showing Symmetric and Asymmetric Load Connections



disrupting the gate drive. In some power circuit layouts it may become necessary to put some part of the R_g impedance in the ground path to impede the flow of ground loop currents. However, in this case improvements in the power circuit layout should be investigated first. In order to maintain uniform switching it is recommended to use relatively small values of series gate resistance. Series gate resistors should never be larger than ten times the value recommended on the data sheet of the module being used. Care must be exercised to make the gate wiring symmetric. In general, the best practice is to minimize the inductance in the gate drive wiring. Use of a printed circuit board mounted directly to the module or short tightly twisted wires of equal length is recommended. Care should be exercised to avoid inductive coupling to the gate drive by keeping the wiring from running parallel to the main circuit current. Figure 4.67 shows a typical turn-off current waveform with imbalance caused by an improper gate drive. In addition to the influences of temperature and gate drive the current balance at turn-on is influenced by the symmetry of the inductance in the power circuit between the main supply capacitors and devices. Figure 4.68 is a circuit showing symmetric versus asymmetric main circuit connections. Figure 4.69 shows a typical turn on waveform with current imbalance caused by asymmetric main circuit inductance. An effective approach to balance the main circuit inductance is minimize the inductance by using laminated bus structures. The current imbalance waveform at turn-on due to improper gate drive also looks like Figure 4.69.

NOTE:
It may be observed that Powerex IGBTs have a negative temperature coefficient of saturation voltage over a wide range of collector currents. This is not a deterrent to parallel operation and, in fact, is an advantage as it yields lower conduction loss at high junction temperature. The homogeneous process characteristics of Powerex IGBTs produce V_{CE}(SAT) characteristics that track as a function of current and temperature such that, once a V_{CE}(SAT) rank is chosen, the parallel devices will share within the given derating factor.

Figure 4.65 Typical Current Imbalance Caused by Assymetric Load Connection

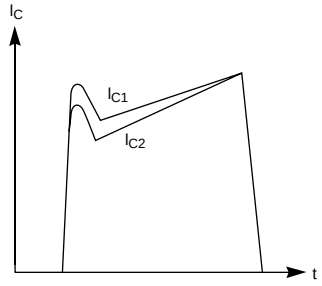


Figure 4.66 Gate Drive Configuration for Paralleled Modules

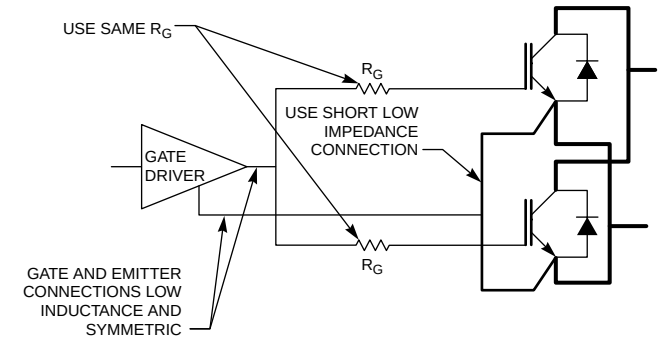


Figure 4.67 Typical Current Waveform Showing Imbalance at Turn-off Due to Improper Gate Drive

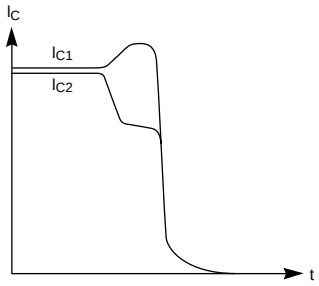


Figure 4.68 Symmetric and Asymmetric Main Circuit Connections

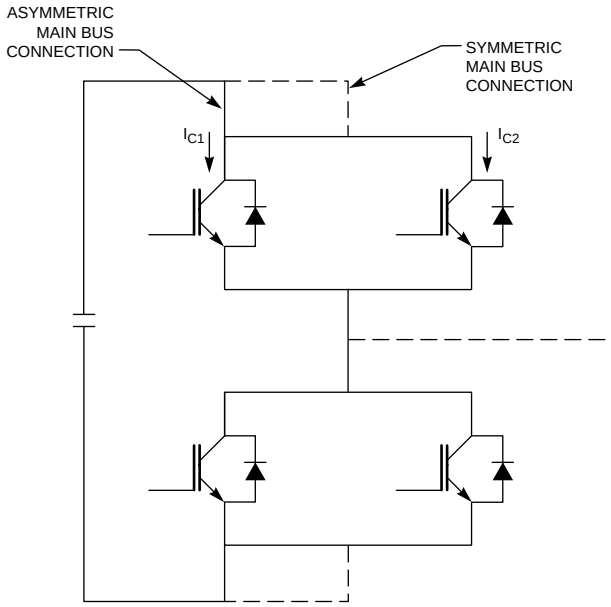


Figure 4.69 Typical Turn-on Waveform with Current Imbalance Caused by Asymmetric Main Circuit Inductance